# PSG5320

## DATA SHEET

## Dual Switching Regulator with On-Demand Power™

## Features

- Configurable On-Demand Power algorithm to adaptively scale regulated output voltage in correlation with monitored system activity
- System sensory interfaces to monitor activity and demand for sub-domains on both regulated voltage domains
- Dual constant-on-time, voltage feed-forward, synchronous step-down controllers
- Wide input voltage range: 6.5V to 24V
- Programmable output voltage range: 2V-3.3V and 3V-5V
- PWM and light-load operation
- Output over and under voltage protection
- Built-in output discharge circuits
- 3.3V and 5V linear regulators for standby power
- 1.2V reference output

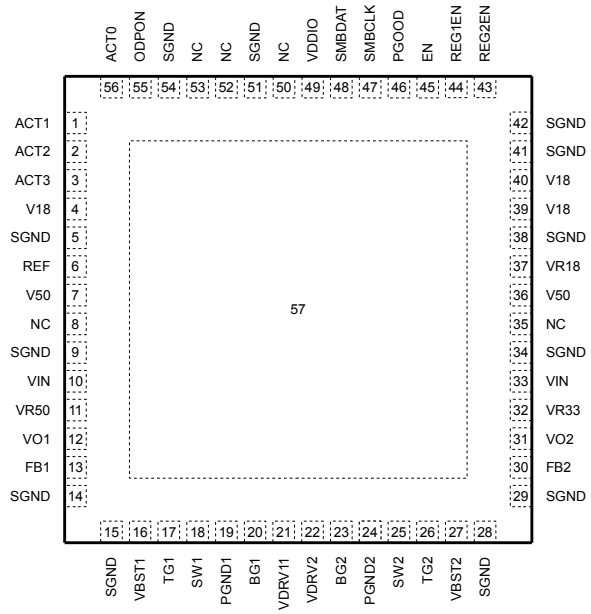
## Description

The PSG5320 is a highly integrated power management unit with two synchronous step-down controllers for system power in notebooks. Independent, programmable interfaces for monitoring activity in the system, coupled with advanced On-Demand Power algorithms, enable the regulated output voltages of the integrated switching regulators to be adaptively scaled in correlation with actual system demand. The real-time tracking of supply voltage to system activity enables maximum system power savings by minimizing the power spent on maintaining worst-case headroom in the power distribution network.

## Applications

- Mobile computers
- Desktop computers
- Servers
- 5V/3.3V supplies
- System power supplies

## Pin Configuration



## Absolute Maximum Ratings (Note 1)

| PARAMETER | VALUE | UNIT |
|---|---|---|
| V50 to SGND | -0.3 to 6 | V |
| VDRV1 to PGND1 and VDRV2 to PGND2 | -0.3 to 6 | V |
| V18 to SGND | -0.3 to 2.0 | V |
| VDDIO to SGND | -0.3 to 6.0 | V |
| VIN to SGND | -0.3 to 30 | V |
| VR18 to SGND | -0.3 to 2.0 | V |
| FB1 and FB2 to SGND | -0.3 to 2.0 | V |
| VBST1 to PGND1 and VBST2 to PGND2 | -0.3 to 30 | V |
| VBST1 to SW1 and VBST2 to SW2 | -0.3 to 6 | V |
| SW1 to PGND1 and SW2 to PGND2 | -2 to 30 | V |
| BG1 to PGND1 and PG2 to PGND2 | -0.3 to 6 | V |
| BG1 to VDRV1 and BG2 to VDRV2 | 0.3 | V |
| TG1 to PGND1 and TG2 to PGND2 | -2 to 30 | V |
| TG1 to SW1 and TG2 to SW2 | -0.3 to 6 | V |
| TG1 to VBST1 and TG2 to VBST2 | 0.3 | V |
| All other pins to SGND | -0.3 to 6.0 | V |
| All other pins to VDDIO | 0.3 | V |
| Maximum Junction Temperature | 125 | °C |

**Note 1** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

# Electrical Characteristics

Unless otherwise noted: $V_{VIN}$ = 15V, $V_{V50}$ = $V_{VDRV}$ = $V_{VDDIO}$ = 5V, $V_{V18}$ = 1.8V, $V_{SGND}$ = $V_{PGND}$ = 0V, $V_{EN}$ = $V_{REG1EN}$ = $V_{REG2EN}$ = 5V, $V_{SMBDAT}$ = $V_{SMBCLK}$ = 5V, $V_{ACT0}$ = $V_{ACT1}$ = $V_{ACT2}$ = $V_{ACT3}$ = 5V, $V_{PGOOD}$ = 5V, VR18 = No Load, VR50 = No Load, VR33 = No Load, $T_A$ = 0°C to 70°C. Typical values are at $T_A$ = 25°C.

### Recommended Operating Conditions

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input Voltage | | 6.5 | | 24 | V |
| $V_{V18}$ | Digital and analog supply voltage | | 1.62 | 1.8 | 1.98 | V |
| $V_{VDDIO}$ | Digital IO supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{V50}$ | Analog supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{VDRV}$ | Bottom gate drive supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{TGDRV}$ | Top gate drive supply voltage | $V_{TGDRV}$ = $V_{VBST}$ - $V_{SW}$ | 4.5 | 5 | 5.5 | V |
| $T_J$ | Operating junction temperature | | 0 | | 70 | °C |

### Power Supplies

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{VIN}$ | Input supply current<br>Core Enabled, Regulators Enabled<br>Core Enabled, Regulators Disabled<br>Disabled | No external load on VR18/VR50/VR33 outputs<br>$V_{EN}$ = $V_{REG1EN}$ = $V_{REG2EN}$ = 5V, $V_{VO1}$ = 5V, $V_{VO2}$ = 3.3V<br>$V_{EN}$ = 5V, $V_{REG1EN}$ = $V_{REG2EN}$ = 0V, VR50 = 5V, VR33 = 3.3V<br>$V_{EN}$ = $V_{REGEN1}$ = $V_{REGEN2}$ = 0V, VR50 = 5V, VR33 = 3.3V | | | <br>50<br>3.9<br>200 | <br>µA<br>mA<br>µA |
| $I_{V18}$ | Digital and analog supply current<br>Enabled<br>Disabled | <br>$V_{EN}$ = $V_{REG1EN}$ = $V_{REG2EN}$ = 5V<br>$V_{EN}$ = $V_{REG1EN}$ = $V_{REG2EN}$ = 0V | | | <br>2.1<br>30 | <br>mA<br>µA |
| $I_{VDDIO}$ | Digital IO supply current | No switching outputs | | | 120 | µA |
| $I_{V50}$ | Analog supply current<br>Enabled<br>Disabled | No load on VR18 output<br>$V_{EN}$ = $V_{REG1EN}$ = $V_{REG2EN}$ = 5V<br>$V_{EN}$ = $V_{REG1EN}$ = $V_{REG2EN}$ = 0V | | | <br>1.6<br>80 | <br>mA<br>µA |
| $I_{VDRV}$ | Bottom gate driver supply current<br>Enabled<br>Disabled | Per channel. All gate drivers are output low<br>$V_{EN}$ = $V_{REG1EN}$ = $V_{REG2EN}$ = 5V<br>$V_{EN}$ = 5V, $V_{REG1EN}$ = $V_{REG2EN}$ = 0V | | | <br>390<br>34 | <br>µA<br>µA |
| $I_{VBST}$ | Top gate driver supply current<br>Enabled<br>Disabled | Per channel. All gate drivers are output low.<br>$V_{EN}$ = $V_{REG1EN}$ = $V_{REG2EN}$ = 5V<br>$V_{EN}$ =5V, $V_{REG1EN}$ = $V_{REG2EN}$ = 0V | | | <br>250<br>150 | <br>µA<br>µA |

### Digital Interface

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SMBDAT, SMBCLK Inputs** | | | | | | |
| $V_{IH}$ | Input high voltage | | | | 2.1 | V |
| $V_{IL}$ | Input low voltage | | 0.8 | | | V |
| $I_{IN(1)}$ | Input current for input high voltage | Input Voltage = 5V (Note 2) | | | -5 | µA |
| $I_{IN(0)}$ | Input current for input low voltage | Input Voltage = 0V (Note 2) | | | 5 | µA |
| **ACT0, ACT1, ACT2, ACT3 Inputs** | | | | | | |
| $V_{IH}$ | Input high voltage | ACTx Low Voltage Input = 0<br>ACTx Low Voltage Input = 1 | | | 1.4<br>0.7 | V |
| $V_{IL}$ | Input low voltage | ACTx Low Voltage Input = 0<br>ACTx Low Voltage Input = 1 | 0.8<br>0.4 | | | V |
| $I_{IN(1)}$ | Input current for input high voltage | Input Voltage = 5V | | | -10 | µA |
| $I_{IN(0)}$ | Input current for input low voltage | Input Voltage = 0V | | | 10 | µA |
| **EN, REG1EN, REG2EN, ODPEN Inputs** | | | | | | |
| $V_{IH}$ | Input high voltage | | | | 2.1 | V |
| $V_{IL}$ | Input low voltage | | 0.8 | | | V |

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{IN(1)}$ | Input current for input high voltage | Input Voltage = 5V | | | -10 | µA |
| $I_{IN(0)}$ | Input current for input low voltage | Input Voltage = 0V | | | 10 | µA |
| **SMBDAT Output** | | | | | | |
| $V_{OL}$ | Low level output voltage | $I_{OL}$ = 2mA | | | 0.4 | V |
| $I_{OH}$ | High level output leakage current | Output Voltage = 5V (Note 2) | | | 5 | µA |
| **PGOOD Output** | | | | | | |
| $V_{OL}$ | Low level output voltage | $I_{OL}$ = 2mA | | | 0.4 | V |
| $I_{OH}$ | High level output leakage current | Output Voltage = 5V | | | 10 | µA |

### Two-Wire Interface (Note 3)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SMB}$ | SMBus clock frequency | | 10 | | 100 | kHz |
| $t_{LOW}$ | SMBus clock low time | Measured from $V_{IL(MAX)}$ to $V_{IL(MAX)}$ | 4.7 | | | µs |
| $t_{HIGH}$ | SMBus clock high time | Measure from $V_{IH(MIN)}$ to $V_{IH(MIN)}$ | 4.0 | | | µs |
| $t_{r,SMB}$ | SMBus rise time | (Note 4) | | | 1 | µs |
| $t_{f,SMB}$ | SMBus fall time | (Note 5) | | | 0.3 | µs |
| $t_{OF}$ | Output fall time | $C_L$ = 400 pF, $I_O$ = 3mA, (Note 5) | | | 250 | ns |
| $t_{TIMEOUT}$ | SMBDAT and SMBCLK time low for reset of SMBus | (Note 6) | 25 | | 35 | ms |
| $t_{SU,DAT}$ | Data setup time | | 250 | | | ns |
| $t_{HD,DAT}$ | Data hold time | | 300 | | | ns |
| $t_{HD,STA}$ | Hold time after (repeated) start condition. After this period, the first clock is generated. | | 4 | | | µs |
| $t_{SU,STO}$ | Stop condition setup time | | 4 | | | µs |
| $t_{SU,STA}$ | Repeated start condition setup time | | 4.7 | | | µs |
| $t_{BUF}$ | Bus free time between stop and start conditions | | 4.7 | | | µs |

### 5MHz Internal Oscillator

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{5MHZ}$ | Internal oscillator frequency | | 4.5 | | 5.5 | MHz |

### Switching Regulators

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Gate Drivers** | | | | | | |
| $R_{TG(UP)}$ | TG driver pull-up on resistance | TG high | | 2.1 | 8 | Ω |
| $R_{TG(DOWN)}$ | TG driver pull-down on resistance | TG low | | 1.5 | 4 | Ω |
| $R_{BG(UP)}$ | BG driver pull-up on resistance | BG high | | 1.4 | 8 | Ω |
| $R_{BG(DOWN)}$ | BG driver pull-down on resistance | BG low | | 0.7 | 4 | Ω |
| $t_{DEAD(TG/BG)}$ | Dead time | TG low to BG high (Note 7) | | 53 | | ns |
| $t_{DEAD(BG/TG}$ | Dead time | BG low to TG high (Note 7) | | 30 | | ns |
| **$V_{OUT}$ Discharge** | | | | | | |
| $I_{DISCHG}$ | $V_{OUT}$ discharge current | $V_{EN}$ = 5V, $V_{REGxEN}$ = 0V, $V_{VOx}$ = 0.5V | 10 | | | mA |
| **Duty and Frequency Control** | | | | | | |
| $t_{ON(1)}$ | On time | $V_{VIN}$ = 20V, VSETx[7:0] = 55h | | 389 | | ns |
| $t_{ON(2)}$ | On time | $V_{VIN}$ = 20V, VSETx[7:0] = 00h | | 410 | | ns |

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{ON(3)}$ | On time | $V_{VIN}$ = 15V, VSETx[7:0] = 55h | | 552 | | ns |
| $t_{ON(4)}$ | On time | $V_{VIN}$ = 15V, VSETx[7:0] = 00h | | 616 | | ns |
| $t_{ON(5)}$ | On time | $V_{VIN}$ = 10V, VSETx[7:0] = 55h | | 979 | | ns |
| $t_{ON(6)}$ | On time | $V_{VIN}$ = 10V, VSETx[7:0] = 00h | | 1195 | | ns |
| $t_{OFF(MIN)}$ | Minimum off time | | | 420 | | ns |
| $t_{DEAD(MAX)}$ | DCM timeout | | | 1026 | 1130 | ns |
| **Softstart** | | | | | | |
| $t_{SS(10)}$ | Softstart time | | 1.2 | | 2.5 | ms |
| **Powergood (PG)** | | | | | | |
| $V_{PG1(L)}$<br>$V_{PG1(H)}$ | PG trip voltage<br>Lower PG trip voltage<br>Upper PG trip voltage | With respect to set regulated voltage $V_{VO1}$ = 4V to 5V<br>$V_{VO1}$ ramping negative<br>$V_{VO1}$ ramping positive | <br>-600<br>300 | | <br>-300<br>600 | <br>mV<br>mV |
| $V_{PG2(L)}$<br>$V_{PG2(H)}$ | PG trip voltage<br>Lower PG trip voltage<br>Upper PG trip voltage | With respect to set regulated voltage $V_{VO2}$ = 2V to 3.3V<br>$V_{VO2}$ ramping negative<br>$V_{VO2}$ ramping positive | <br>-450<br>150 | | <br>-150<br>450 | <br>mV<br>mV |
| $t_{PGDEL}$ | PG delay | Entering PG window | 115 | 130 | 145 | µs |
| **Over Voltage Protection (OVP)** | | | | | | |
| $V_{OVP1(F)}$ | Channel 1 Fixed OVP trip voltage | | 5.6 | | 5.9 | V |
| $V_{OVP1(D)}$ | Channel 1 Dynamic OVP trip voltage | With respect to set regulated voltage $V_{VO1}$ = 4V to 5V | 0.8 | | 1.4 | V |
| $V_{OVP2(F)}$ | Channel 2 Fixed OVP trip voltage | | 3.45 | | 3.65 | V |
| $V_{OVP2(D)}$ | Channel 2 Dynamic OVP trip voltage | With respect to set regulated voltage $V_{VO2}$ = 2V to 3.3V | 0.5 | | 1.0 | V |
| $t_{OVPDEL}$ | OVP prop delay | | | 10 | | µs |
| **Under Voltage Protection (UVP)** | | | | | | |
| $V_{UVP}$ | UVP trip voltage | | 1.08 | | 1.32 | V |
| $t_{UVPDEL}$ | UVP prop delay | | 25 | | 40 | µs |
| $t_{UVPEN}$ | UVP enable delay | From rising edge of REGxEN | 1.9 | | 3.8 | ms |
| **Current Sense** | | | | | | |
| $V_{OCP(OFF)(6)}$ | Over current protection offset voltage | OCPROGx[3:0]=6h | | 33 | | mV |
| $TC_{OCP(6)}$ | Over current protection temperature coefficient | OCPROGx[3:0]=6h | | 118 | | µV/°C |
| $V_{OCP(OFF)(8)}$ | Over current protection offset voltage | OCPROGx[3:0]=8h | | 41 | | mV |
| $TC_{OCP(8)}$ | Over current protection temperature coefficient | OCPROGx[3:0]=8h | | 147 | | µV/°C |
| $V_{OCP(OFF)(A)}$ | Over current protection offset voltage | OCPROGx[3:0]=Ah | | 50 | | mV |
| $TC_{OCP(A)}$ | Over current protection temperature coefficient | OCPROGx[3:0]=Ah | | 187 | | µV/°C |
| $V_{OCP(OFF)(C)}$ | Over current protection offset voltage | OCPROGx[3:0]=Ch | | 59 | | mV |
| $TC_{OCP(C)}$ | Over current protection temperature coefficient | OCPROGx[3:0]=Ch | | 229 | | µV/°C |
| $V_{ZC}$ | Zero cross detection comparator offset | | -5 | | 8 | mV |
| **Programmable Output Voltage** | | | | | | |
| $V_{PROG(MAX)}$ | Maximum programmable output voltage | | 4.8 | | | V |
| $V_{PROG(MIN)}$ | Minimum programmable output voltage | | | | 4 | V |
| $V_{PROG(ERROR)}$ | Programmable output voltage error | VSETx[7:0] = 00h to 55h, V50 = 4.5V to 5.5V, V18 = 1.62V to 1.98V | | 14.95 | 120 | mV |

## 1.2V Reference

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{VREF}$ | VREF reference output voltage | -0.5µA < $I_{VREF}$ < 100µA | 1.182 | | 1.218 | V |

### 5.0V Linear Regulator

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{VR50}$ | 5.0V linear regulator output voltage | VO1 = 0V, $I_{LDO50}$ < 100mA | 4.5 | | 5.5 | V |
| $V_{50SW}$ | Bypass switch threshold | Switch output from VR50 to VO1 and disable VR50 | 4.58 | | 4.68 | V |
| $V_{50SWHY}$ | Bypass switch hysteresis | | 0.05 | | 0.08 | V |
| $R_{50SW}$ | 5.0V switch on resistance | VO1 = 5V | | | 3 | Ω |

### 3.3V Linear Regulator

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{VR33}$ | 3.3V linear regulator output voltage | VO2 = 0V, $I_{LDO33}$ < 100mA | 2.97 | | 3.63 | V |
| $V_{33SW}$ | Bypass switch threshold | Switch output from VR33 to VO2 and disable VR33 | 3.05 | | 3.15 | V |
| $V_{33SWHY}$ | Bypass switch hysteresis | | 0.05 | | 0.08 | V |
| $R_{33SW}$ | 3.3V switch on resistance | VO2 = 3.3V | | | 4 | Ω |

### 1.8V Linear Regulator

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{VR18}$ | 1.8V LDO output voltage | 0 < $I_{VR18}$ < 5mA | 1.71 | | 1.98 | V |

**Note 2** Characteristic tested at 25°C. Temperature limits established by characterization and are not production tested.

**Note 3** Unless otherwise noted, these specifications apply for load capacitances on SMBus lines = 80pF. The switching characteristics of the PSG5320 fully meet or exceed the published specifications of the SMBus version 2.0.

**Note 4** The rise time is measured from ($V_{IL(MAX)}$ - 0.15V) to ($V_{IH(MIN)}$ + 0.15V).

**Note 5** The fall time is measured from ($V_{IH(MIN)}$ + 0.15V) to ($V_{IL(MAX)}$ – 0.15V).

**Note 6** Exceeding $t_{TIMEOUT}$ will reset the PSG5320 SMBus state machine, therefore setting SMBDAT and SMBCLK pins to a high impedance state.

**Note 7** Delay times are measured using 50% levels.

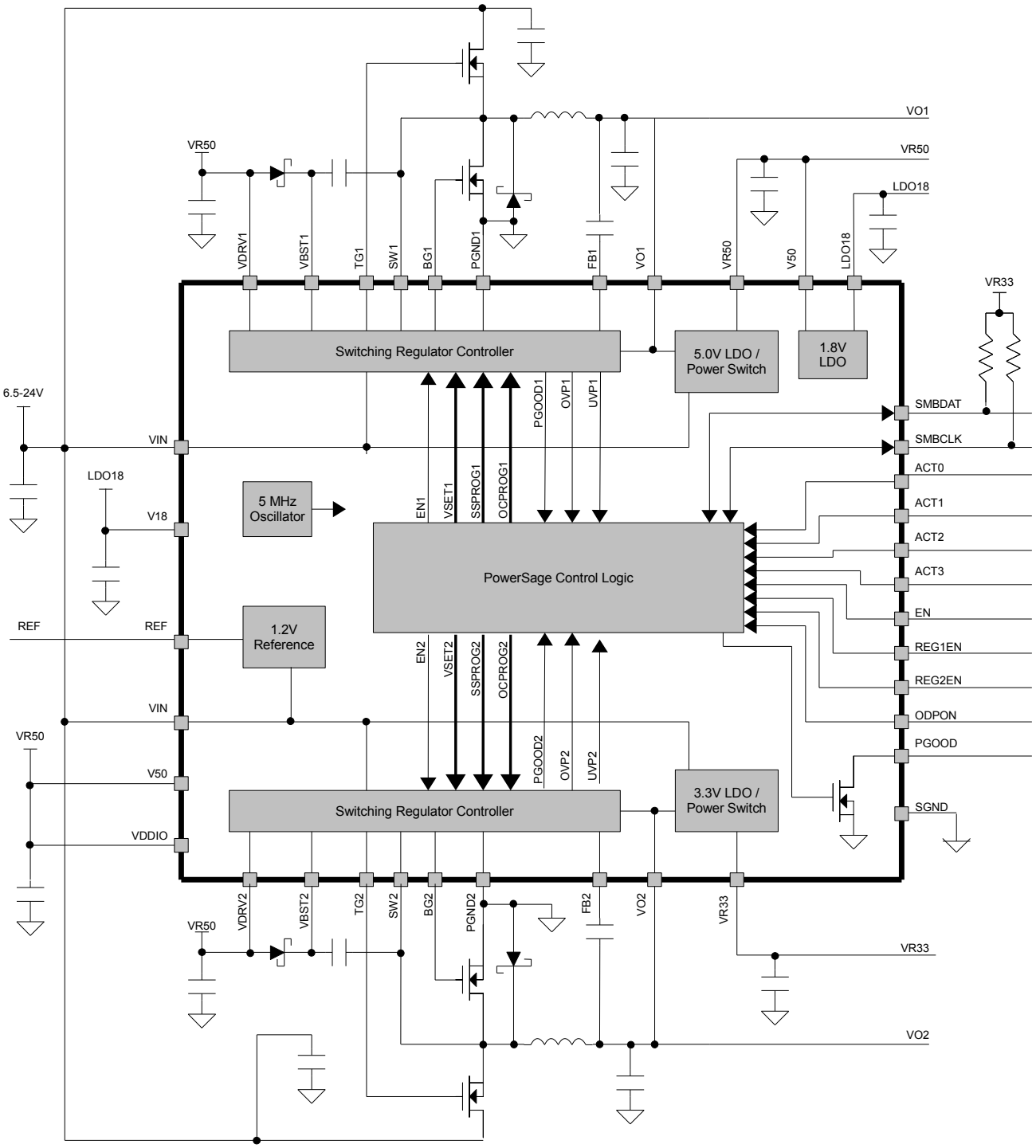
**Note 8** Guaranteed by design.

## Pin Functions

| NAME | PIN | IO (Note 9) | DESCRIPTION |
|---|---|---|---|
| V18 | 4, 39, 40 | P | 1.8V power supply for both digital and analog circuitry. Decouple each pin to SGND with a capacitor. |
| VDDIO | 49 | P | IO power supply. Decouple to SGND with a capacitor. This is the input supply for digital IO drivers and receivers. |
| V50 | 7, 36 | P | 5V power supply for analog circuitry. Decouple each pin to SGND with a capacitor. |
| VIN | 10 | P | High voltage sense input. Decouple to SGND with a capacitor. |
| SGND | 5, 9, 14, 15, 28, 29, 34, 38, 41, 42, 51, 54 | P | Small signal ground. All small signal components should connect to this ground. Connect SGND to PGND1,2 at one point. Pin 57 is the exposed pad |
| PGND1,2 | 19, 24 | P | Channel 1 and 2 power grounds. Connect these closely to the appropriate sources of the bottom external N-channel MOSFETs and the negative terminal of the VDRV1,2 decoupling capacitors. Connect PGND1,2 to SGND at one point. |
| VDRV1,2 | 21, 22 | P | Channel 1 and 2 bottom gate driver supply. Decouple to its respective PGND with a capacitor. |
| VR50 | 11 | PO | Internal 5.0V regulator output. Decouple to SGND with a capacitor, |
| VR33 | 32 | PO | Internal 3.3V regulator output. Decouple to SGND with a capacitor, |
| VR18 | 37 | PO | Internal 1.8V linear regulator output. Decouple to SGND with a capacitor. This output can be connected to V18 as the 1.8V supply. |
| REF | 6 | AO | Internal 1.2V reference output |
| VO1,2 | 12, 31 | A | Channel 1 and 2 output voltage remote sense inputs. |
| FB1,2 | 13, 30 | A | Channel 1 and 2 output voltage feedback. Connection point for external ripple injection circuitry or leave floating. |
| ACT0,1,2,3 | 1-3, 56 | I | On-Demand Power inputs. Logic threshold level and polarity are programmable. Connect directly to SGND if not used. Do not leave floating. |
| SMBDAT | 48 | IOD | SMBus data input/output. The PSG5320 is configured as an SMBus device. |
| SMBCLK | 47 | IOD | SMBus clock input. The PSG5320 is configured as an SMBus device. |
| PGOOD | 46 | OD | Power good indicator output. This open-drain output is pulled to ground when either the channel 1 or channel 2 regulated output voltages leave the regulation window. Each regulator has a fixed 512us power good delay. Each channel has an additional programmable delay and mask. |
| EN | 45 | I | Enable input. A logic low disables the switching regulators and forces the PSG5320 into a low-power standby mode. A logic high enables the PSG5320 and the regulator operation is dependent on the REG1EN and REG2EN inputs. Connect directly to VDDIO if not used. Do not leave this pin floating. The output discharge circuits are disabled when EN is a logic low. |
| REG1EN | 44 | I | Channel 1 regulator enable input. A logic low disables the channel 1 regulator and activates the output discharge circuit. When the input is a logic high, the operational state of the channel 1 regulator is dependent on the internal channel 1 regulator enable bit. Connect directly to VDDIO if not used. Do not leave this pin floating. |
| REG2EN | 43 | I | Channel 2 regulator enable input. A logic low disables the channel 2 regulator and activates the output discharge circuit. When the input is a logic high, the operational state of the channel 2 regulator is dependent on the internal channel 2 regulator enable bit. Connect directly to VDDIO if not used. Do not leave this pin floating. |
| ODPON | 55 | I | On-Demand Power enable override. A logic high overrides programmable settings for ODP enable for both channels and forces the On-Demand Power to be enabled. |
| VBST1,2 | 16, 27 | P | Boosted floating driver supplies for the channel 1 and 2 top gate drivers. |
| SW1,2 | 18, 25 | A | Channel 1 and 2 switch node connections to power inductors. |
| TG1,2 | 17, 26 | AO | Channel 1 and 2 top gate driver outputs. |
| BG1,2 | 20, 23 | AO | Channel 1 and 2 bottom gate driver outputs. |
| NC | 8, 35, 50, 52, 53 | X | No Connect. These pins should be left floating. |

**Note 9** P = Power, A = Analog, I = Input, O = Output, OD = Open Drain, IOD = Bidirectional Open Drain, X = Unconnected

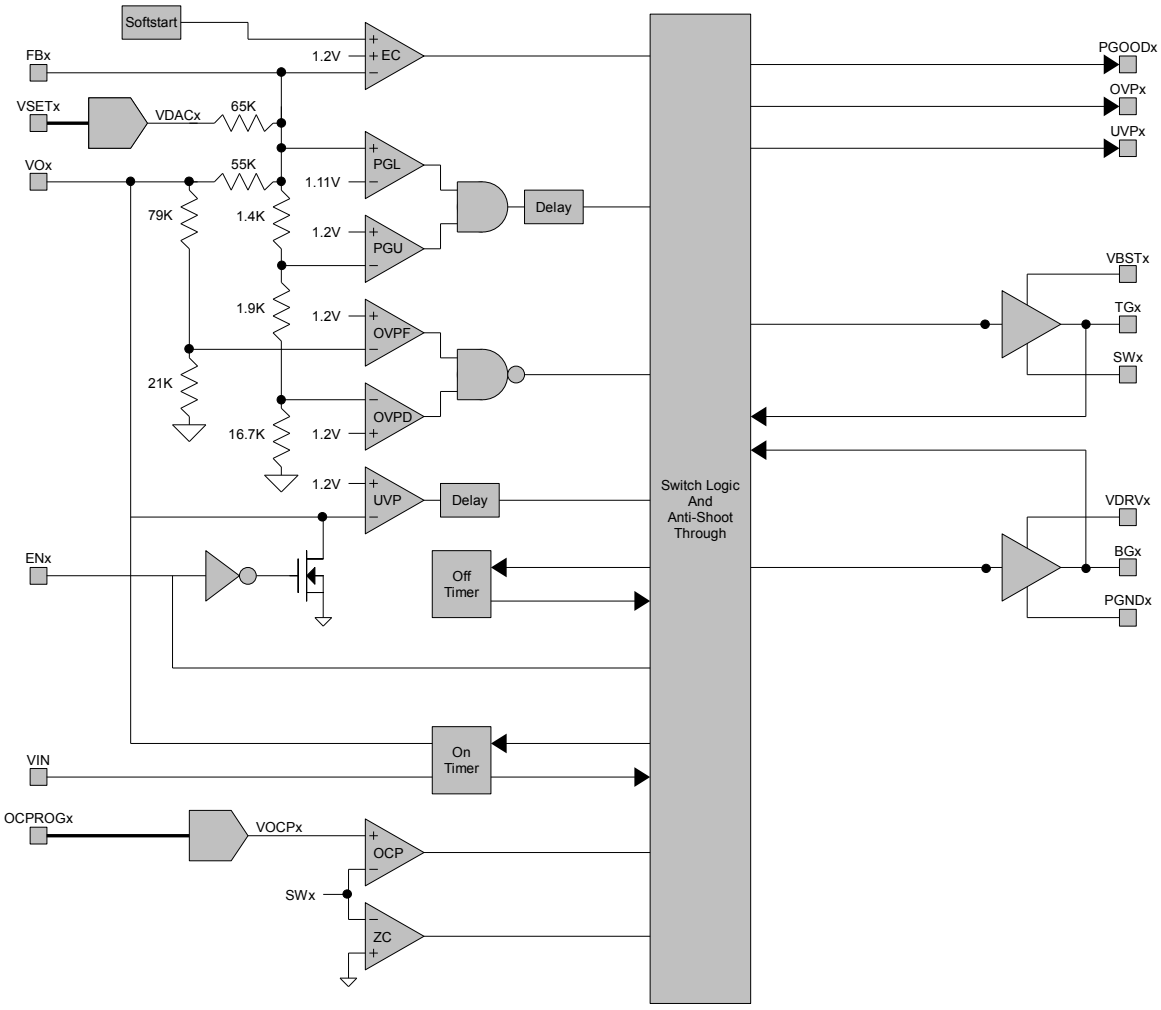
## 1 Functional Diagram




## 2 Synchronous PWM controller

This is a high efficiency constant on time input voltage feed-forward step-down synchronous PWM controller. The controller automatically switches between continuous conduction mode (CCM) and discontinuous conduction mode (DCM) depending on the average inductor current. In CCM, the top external MOSFET is turned on when the error comparator shows that the output voltage is in error. The top external MOSFET remains on for a fixed amount of time that is dependent on the input and output voltage relationship. When the top external MOSFET is turned off, the bottom external MOSFET is turned on until the inductor current is less than the valley current limit and the error comparator shows that output voltage is in error.

In DCM, the inductor current is not allowed to reverse. Therefore, the bottom MOSFET is turned off when the inductor current reaches zero. Both the top and bottom external MOSFETs remain off until the top external MOSFET is turned on when the error comparator shows that the output voltage is in error. During the time that both external MOSFETs are turned off, the output voltage is supplied by the output capacitor.




## 2.1 On-Time Control

The on-time of the PWM controller is dynamically adjusted on a cycle-by-cycle basis to maintain a constant ripple current in the power inductor. The input and output voltage of the switching regulator is monitored to adapt the period of a one-shot timer that sets the on-time of the controller. The typical on-time for channel 1 and channel 2 are:

$$t_{ONx} = \frac{5.83\,\mu Vs}{V_{VIN} - V_{VOx}}$$

## 2.2 DCM Operation

During light load, the PWM controller enters DCM to maintain high conversion efficiency. DCM is entered when the inductor valley current reaches zero and the bottom external MOSFET is turned off to prevent the inductor current from reversing. This decreases the effective switching frequency of the controller and reduces conversion losses in the MOSFET drivers. When both the top and bottom external MOSFETs are off, the output voltage is maintained by the output capacitance. Once the light load discharges the output capacitance to the point where the error comparator detects that the output voltage is in error, a new switching cycle is started by tuning on the top external MOSFET. The on-time is not effected. The load current where the controller transitions between CCM and DCM is:

$$I_{OUTx} = \frac{1}{2}\left(\frac{V_{VIN} - V_{VOx}}{L_x}\right)t_{ONx}$$

When operating in DCM, the effective switching frequency is dependent on the load current. The approximate switching

frequency is:

$$f = \frac{I_{OUTx}}{\left(\frac{V_{VIN}-V_{VOx}}{2L_x}\left(t_{ONx}+\frac{V_{VIN}-V_{VOx}}{V_{VOx}}\right)\right)}$$

The maximum time both external MOSFETs can remain off while in DCM mode is limited to 1026μs. In the event of a DCM timeout, the bottom external MOSFET is turned on first for the minimum off-time to recharge the boost capacitor. Subsequently, the top external MOSFET is only turned on if the error comparator detects that the output voltage is in error.

### 2.3 External Ripple Injection

External ripple injection is used to couple extra output ripple to the error comparator through the FBx pin. Correctly choosing this capacitor can minimize jitter in the switching frequency and allow for reduced output ripple. Internally there is a 20KOhm equivalent series resistance. The circuit should be designed to pass frequencies near and above 50kHz. A band-pass filter that passes frequencies between 50k and 5MHz will be optimal if there will be noisy signals in close proximity to the PSG5320. A simple high pass filter can be designed on the following formula:

$$f = \frac{1}{2\times\pi\times R\times C}$$

A 180pF series capacitor from VOx to FBx is a reasonable circuit for the external ripple injection for most conditions.

### 2.4 MOSFET Drivers

Both the top and bottom MOSFET drivers are designed to drive N-channel external power MOSFETs. The bottom MOSFET driver pulls BGx down to PGNDx to turn off the external MOSFET, and it pulls BGx up to VDRVx to turn on the external MOSFET. Likewise, the top external MOSFEST driver pulls TGx down to SWx to turn off the external MOSFET, and it pulls TGx up to VBSTx to turn on the external MOSFET. The combined power dissipation of both MOSFET drivers in a single PWM controller channel attributed to switching events is:

$$P_{DISx} = V_{VDRVx}\times f_x\times\left(Q_{Tx}+Q_{Bx}\right)$$

where $f_x$ is the switching frequency, $Q_{Tx}$ is the gate charge of the top external MOSFET, and $Q_{Bx}$ is the gate charge of the bottom external MOSFET.

The top MOSFET driver has a floating power supply $V_{VBSTx}$ - $V_{SWx}$ that is derived from the 5V supply using a boost capacitor and boost diode. The boost capacitor is recharged through the boost diode from the 5V supply when ever the bottom external MOSFET is turned on and SWx is pulled to PGND.

### 2.5 Anti-Shoot Through Circuitry

In a synchronous pwm topology, it is possible to get shoot-through current from VIN to PGND when both the top and bottom external MOSFETs are fully or partially conducting. To prevent this, a dead time where both MOSFETs are off is internally generated by adding a delay from the turn off of the top external MOSFET to the turn on of the bottom external MOSFET and from the turn off of the bottom external MOSFET to the turn on of the top external MOSFET. The voltage and discharge current of both the top and bottom external MOSFETs are monitored to dynamically optimize the driver dead time and increase conversion efficiency.

### 2.6 Start-Up

The channel 1 PWM controller is enabled when both the EN and REG1EN pins are driven high. Likewise, the channel 2 PWM controller is enabled when both the EN and REG2EN pins are driven high. When enabled, there is a brief delay while the internal analog circuitry is powered-on and stabilized. Next, an internal DAC, one per channel, linearly ramps the error comparator reference voltage from 0V to VREF. This forces the regulated output voltage of the enabled channel to linearly increase from 0V to the final programmed output voltage in 1.5ms.

### 2.7 Shutdown

The channel 1 PWM controller is disabled when either the EN or REG1EN pins are driven low. Likewise, the channel 2 PWM controller is disabled when either the EN or REG2EN pins are driven low. When disabled, the internal analog circuitry of the PWM controller is forced into a low power mode.

### 2.8 Output Discharge Circuitry

A 10mA minimum output discharge current sink is connected through VOx for each channel. The output discharge is active when the respective REGENx pins are driven low. The output discharge circuitry is not active when EN is driven low.

## 2.9 Powergood

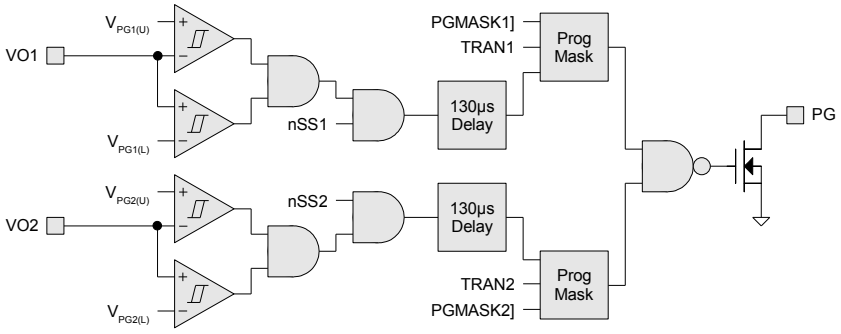
The PGOOD pin is an open-drain output that indicates if the output voltages of the PWM controllers, measured at pins VO1 and VO2, are within regulation. In fixed output voltage operation, the PGOOD pin is high impedance if both regulator outputs are within regulation, and the PGOOD pin is pulled to ground if either regulator output is out of regulation. Additionally, the PGOOD pin is pulled low if either channel is disabled or operating in soft-start. The power good regulation window is defined in the Electrical Characteristics table.

To minimize the effect of noise on the VO1 and VO2 pins, there is an internal fixed 130µs delay on the PGOOD output from both channels. Thus, VO1 or VO2 must be inside the regulation window for at least 130µs before the PGOOD pin becomes high impedance. However, the PGOOD pin will be pulled low immediately after VO1 and VO2 leave the regulation window.

During controlled output voltage transitions, a programmable masking of the PGOOD signal is enabled. While the On-Demand Power™ controller is ramping either VSET control voltage from one fixed voltage to a new fixed voltage, the PGOOD pin will retain its state previous to the beginning of an output voltage transition until the output voltage is complete. Thus, if the PGOOD pin was pulled low at the beginning of a voltage transition, the PGOOD pin will remain pulled low throughout the entire output voltage transition, even if the transition event causes both output voltages to enter the regulation window. Likewise, if the PGOOD pin was high impedance at the beginning of a voltage transition, the PGOOD pin will remain high impedance throughout the entire output voltage transition, event if the transition event cause one of the output voltages to leave the regulation window. The programmable mask during output voltage transitions enable the On-Demand Power™ controller to adjust the programmed output voltage VSET at a rate faster than the output of the PWM controllers can respond without inadvertently causing the PGOOD pin to be pulled low.

Furthermore, the programmable mask can be optionally extended for a programmable time period past the completion of an output voltage transition event. This feature allows the PWM controller output voltage some time to settle within the regulation window after a voltage transition occurs. This can be important when the output voltage step is large and/or the slew rate of VSET is high. The programmable mask is set through the ODPxPGBLANK register which is counted based off of the internal 5MHz clock. The maximum ODPxPGBLANK setting is 51µS.

The complete powergood logic is shown below. nSS1 and nSS2 are low when the respective PWM controller is operating in softstart mode. TRAN1 and TRAN2 indicate if VSET for the respective switching regulator is transitioning. PGMASK1 and PGMASK2 set the programmable mask time period.




**Powergood logic**

## 2.10 Output Voltage Programming

The regulated output voltage of the PWM controllers is controlled with an 8-bit DAC that is programmed by the On-Demand Power™ controller. Some of the upper DAC codes are unavailable due to the manufacturing trim process but the full range of supported voltages are available on every chip. The following equations represent the transfer characteristic between the DAC codes used in the VMAN and On-Demand Power™ state voltage registers.

$$V_{VO1} = 5.1 - \left[2.35\frac{VSET1[7:0]}{256}\right]; \approx 9.2\frac{mV}{bit}$$

$$V_{VO2} = 3.4 - \left[1.55\frac{VSET2[7:0]}{256}\right]; \approx 6.1\frac{mV}{bit}$$

## 2.11 Over Current Protection

Over current protection is provided by monitoring the drain-to-source voltage across the bottom external MOSFET when it is turned on. As long as the sensed voltage drop is greater than the programmed voltage threshold, the bottom external MOSFET is forced to remain on. This effectively limits the maximum value of the power inductor valley current.

The channel 1 and 2 over current protection limits are independently programmed with the OCPROGx bits over the SMBus

interface. The voltage threshold is temperature compensated to match the temperature dependency of the bottom external MOSFET. The programmed voltage threshold is:

$$V_{THx} = 0.37893(OCPROGx+1)((4.94\times10^{-5})T_J+0.01196)$$

For improved accuracy, there should be a good thermal connection between the MOSFET and the PSG5320.

### 2.12 Output Over and Under Voltage Protection

The output voltage of the PWM controllers is sensed at the VO1 and VO2 pins. If the sensed voltage exceeds either the fixed output over voltage threshold or the dynamic over voltage threshold, the bottom external MOSFET of the PWM controller experiencing the over voltage conditions is turned on to discharge the output capacitance and return the output voltage to safe operating level. Once the over voltage condition is no longer sensed, the PWM controller resumes normal operation.

When the sensed output voltage drops below the under voltage threshold, the PWM controller experiencing the under voltage condition is automatically disabled. The EN pin or REGxEN pin associated with the disabled PWM controller must be toggled to clear the under voltage condition. This response is desired because an under voltage condition will follow an output short circuit that triggers the over current protection circuitry. This protects the PWM controller and associated circuitry against an output short circuit.

### 2.13 UVLO Protection

All power supplies are monitored to ensure they are of suitable voltage before the PWM controllers are enabled.

## 3 Switching Regulator Circuit Design

### 3.1 Inductor Selection

The maximum load current and inductor ripple current determine the value of the inductor. The value of the inductor ripple current $\Delta I_L$ can be calculated with input voltage $V_{IN}$, output voltage $V_{Ox}$, and on time $t_{ONx}$:

$$\Delta I_L = t_{ONx}\left(\frac{V_{VIN}-V_{VOx}}{L}\right)$$

Since the on-time of the PWM controller is adjusted to maintain a constant ripple current, $\Delta I_L$ is determined solely by the inductance value. A lower ripple current improves efficiency by reducing losses in the inductor and ESR losses in the input and output capacitors at the cost of a physically larger inductor. A $\Delta I_L$ that is 25% to 50% of $I_{LOAD(MAX)}$ is reasonable for balancing efficiency and inductor size.

An inductor should be selected to have the lowest possible DC resistance to maximize efficiency. Care must be taken to not saturate at the peak inductor current which can be determined by:

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{\Delta I_L}{2}$$

### 3.2 Output Capacitor Selection

Equivalent series resistance (ESR) is a dominant qualification for output capacitor selection. Specialty polymer capacitors, such as Sanyo POSCAP, are recommended due to high ripple current capability and low ESR at operation frequencies.

Output capacitance should be selected to provide an acceptable output voltage ripple $\Delta V_{VOx}$ which can be determined by the ESR and magnitude of the output capacitor. The capacitance must be sufficiently large for stability, however the capacitance value relates to the increasing physical size needed to decrease ESR. Consequently, the selection of $C_{OUT}$ is primarily driven by ESR and can be found by:

$$ESR \le \frac{\Delta V_{VOx}}{\Delta I_L}$$

### 3.3 Input Capacitor Selection

Select the input capacitors based on the expected maximum input ripple RMS current. This current varies with the load, input voltage, and phase of both PWM controllers. Since each channel operates at different frequencies, the worst-case phase causing an overlap in current pulses occurs over a short time duration. The maximum input ripple RMS current for a single output channel occurs at maximum load and can be estimated by:

$$I_{RMS(MAX)} \approx \frac{I_{LOAD(MAX)}}{V_{VIN}}\left[(V_{VOx})(V_{VIN}-V_{VOx})\right]^{1/2}$$

### 3.4 MOSFET Selection

The top and bottom MOSFET should be chosen for low $R_{DS(ON)}$ for increased efficiency, however this must be weighed with

increased gate capacitance which increases switching losses. Switching losses are increased in the top MOSFET at high input voltages.

The bottom MOSFET should be placed in parallel with a Schottky diode. Many manufacturers provide a single package device for the MOSFET and diode specifically designed for switching regulators.

# 4 VR50 and VR33 Linear Regulators

Two 100mA linear regulators, 5V and 3.3V, are provided. These regulators are designed to supply system standby power when the synchronous regulators are not operating. External decoupling capacitors are required for each regulator. These capacitors may be ceramic and should be at least 22uF for each regulator.

In typical applications, the 5V linear regulator provides power to the analog and digital circuitry in the PSG5320 when connected to V50, VDDA, and VDRV.

## 4.1 VR50 Bypass Switch

When the voltage at VO1 is higher than 4.6V and the channel 1 power good is set, the VR50 linear regulator is put into standby and the VR50 output is connected to VO1 by an internal bypass switch. Comparator hysteresis and switch delay ensure stable operation.

## 4.2 VR33 Bypass Switch

When the voltage at VO2 is higher than 3.1V and the channel 2 power good is set, the VR33 linear regulator is put into standby and the VR33 output is connected to VO2 by an internal bypass switch. Comparator hysteresis and switch delay ensure stable operation.

# 5 1.8V Linear Regulator

One 1.8V, 25mA linear regulator is provided. This regulator powers the internal digital logic of the PSG5320 though power pins V18 and may be used for light loads in the system. An external decoupling capacitor is required between VR18 and SGND. This capacitor may be ceramic and should be at least 4.7uF.

# 6 On-Demand Power™ Operation

PSG5320 internal registers are programmable via SMBUS to control On-Demand Power™ (ODP) circuitry. Activity on each domain is monitored by programmed activity inputs. When the ODPEN bit of ODPxCON is set or the ODPON pin is held high, the corresponding output voltage will be managed based on configuration settings and signals gathered from ACTx sensing inputs.

## 6.1 Output Voltage

Output voltage will vary based on system demand, managed by On-Demand Power™ algorithms. Channel 1 has been optimized to supply 5Vx and Channel 2 the 3.3Vx supply in notebook computers

## 6.2 ACTx Inputs

ACT0, 1, 2, 3 are system control inputs to the On-Demand Power™ algorithm. A logic high signal on these pins indicates a transition to a higher power state on a output channel. Routing of these input signals to a ODP channel is done through configuration registers ODPxACTx. Each ACT input can be used to control one or both ODP channel, independently controlling the input to any power state.

The ACT inputs can be independently selected for standard or low voltage digital input can be inverted globally and independently though the ACTCON register. $V_{IH}$ and $V_{IL}$ levels for standard and low voltage inputs are defined in the electrical characteristics.

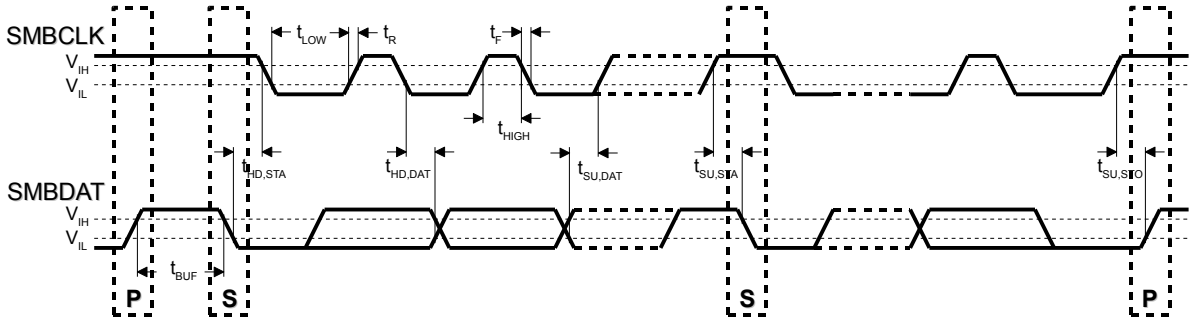
## 6.3 ODPON Input

Setting the ODPON input to high overrides the ODPxCON ODPEN bit and forces both ODP channels to ODP-enable. The default ODP settings for each channel have been designed to operate an average notebook computer system power supplies. Therefore, On-Demand Power™ operation with baseline settings can be utilized in-system without configuration register writes. Toggling ODPON will not cause any changes to register settings

# 7 Two Wire Interface

The PSG5320 serial interface is compatible with the SMBus 2.0 specification. SMBCLK is the serial clock input and SMBDAT is the bidirectional serial data. PSG5320 is configured as a slave and has a fixed 7-bit slave address of 0x61. PSG5320 supports 'read byte', 'write byte', and 'block write' as described by the SMBus specification.

## 7.1 Timing Diagram



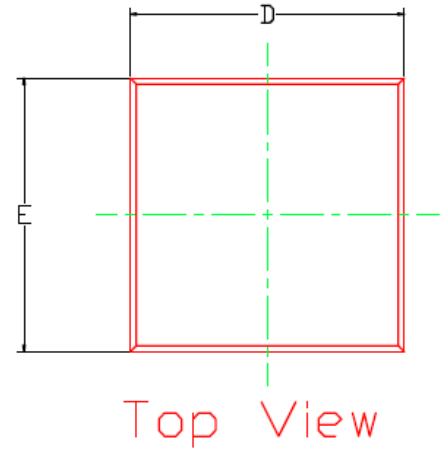

## 7.2 Address Map

| ADDRESS | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 | NAME | DEFAULT VALUE |
|---|---|---|---|---|---|---|---|---|---|---|
| 00H | Product ID | | | | | | | | PID | 0x03 |
| 01H | Reserved | | | | | | | | RESERVED | |
| 02H | Reserved | | | | | | | | RESERVED | |
| 03H | Reserved | | | | | | | | RESERVED | |
| 04H | Input Invert | | | | Low Voltage Input | | | | ACTCON | 0x11 |
| 05H-0AH | Reserved | | | | | | | | RESERVED | |
| 10H | Reserved | | | | REGEN STAT | PGSTAT | OVP STAT | UVP STAT | VREG1STAT | 0x00 |
| 11H | Reserved | | | | | | | | RESERVED | 0x00 |
| 12H | Reserved | ODP_STATE | | | Reserved | PGOOD_ MASK | REG_EN | ODP_EN | ODP1CON | 0x00 |
| 13H | ODP 1 Static Output Voltage | | | | | | | | ODP1VOUT0 | 0x00 |
| 14H | ODP 1 State 1 Output Voltage | | | | | | | | ODP1VOUT1 | 0x00 |
| 15H | ODP 1 State 2 Output Voltage | | | | | | | | ODP1VOUT2 | 0x00 |
| 16H | ODP 1 State 3 Output Voltage | | | | | | | | ODP1VOUT3 | 0x00 |
| 17H | ODP 1 State 4 Output Voltage | | | | | | | | ODP1VOUT4 | 0x00 |
| 18H | ODP 1 Timeout 0 [7:0] | | | | | | | | ODP1TOUT0_0 | 0x00 |
| 19H | ODP 1 Timeout 0 [15:8] | | | | | | | | ODP1TOUT0_1 | 0x00 |
| 1AH | ODP 1 Timeout 0 [23:16] | | | | | | | | ODP1TOUT0_2 | 0x00 |
| 1BH | ODP 1 Timeout 1 [7:0] | | | | | | | | ODP1TOUT1_0 | 0x00 |
| 1CH | ODP 1 Timeout 1 [15:8] | | | | | | | | ODP1TOUT1_1 | 0x00 |
| 1DH | ODP 1 Timeout 1 [23:16] | | | | | | | | ODP1TOUT1_2 | 0x00 |
| 1EH | ODP 1 Timeout 2 [7:0] | | | | | | | | ODP1TOUT2_0 | 0x00 |
| 1FH | ODP 1 Timeout 2 [15:8] | | | | | | | | ODP1TOUT2_1 | 0x00 |
| 20H | ODP 1 Timeout 2 [23:16] | | | | | | | | ODP1TOUT2_2 | 0x00 |
| 21H | ODP 1 Timeout 3 [7:0] | | | | | | | | ODP1TOUT3_0 | 0x00 |
| 22H | ODP 1 Timeout 3 [15:8] | | | | | | | | ODP1TOUT3_1 | 0x00 |
| 23H | ODP 1 Timeout 3 [23:16] | | | | | | | | ODP1TOUT3_2 | 0x00 |
| 24H | Prescale | | | | ODP 1 Rising Slew Rate 0 | | | | ODP1SLEWUP0 | 0x00 |
| 25H | Prescale | | | | ODP 1 Rising Slew Rate 1 | | | | ODP1SLEWUP1 | 0x00 |
| 26H | Prescale | | | | ODP 1 Rising Slew Rate 2 | | | | ODP1SLEWUP2 | 0x00 |
| 27H | Prescale | | | | ODP 1 Rising Slew Rate 3 | | | | ODP1SLEWUP3 | 0x00 |
| 28H | Prescale | | | | ODP 1 Falling Slew Rate 0 | | | | ODP1SLEWDOWN0 | 0x00 |
| 29H | Prescale | | | | ODP 1 Falling Slew Rate 1 | | | | ODP1SLEWDOWN1 | 0x00 |
| 2AH | Prescale | | | | ODP 1 Falling Slew Rate 2 | | | | ODP1SLEWDOWN2 | 0x00 |

| ADDRESS | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 | NAME | DEFAULT VALUE |
|---|---|---|---|---|---|---|---|---|---|---|
| 2BH | Prescale | | | | ODP 1 Falling Slew Rate 3 | | | | ODP1SLEWDOWN3 | 0x00 |
| 2CH | Regulator 1 PGOOD Blank Time | | | | | | | | ODP1PGBLANK | 0x00 |
| 2DH | ODP 1 Input Select 1 | | | | ODP 1 Input Select 0 | | | | ODP1ACT0 | 0xFF |
| 2EH | Reserved | | | | ODP 1 Input Select 2 | | | | ODP1ACT1 | 0x0F |
| 2FH-3FH | Reserved | | | | | | | | RESERVED | |
| 40H | Reserved | | | | REGEN STAT | PGSTAT | OVP STAT | UVP STAT | VREG2STAT | 0x00 |
| 41H | Reserved | | | | | | | | RESERVED | 0x00 |
| 42H | Reserved | ODP_STATE | | | Reserved | PGOOD_ MASK | REG_EN | ODP_EN | ODP2CON | 0x00 |
| 43H | ODP 2 Static Output Voltage | | | | | | | | ODP2VOUT0 | 0x00 |
| 44H | ODP 2 State 1 Output Voltage | | | | | | | | ODP2VOUT1 | 0x00 |
| 45H | ODP 2 State 2 Output Voltage | | | | | | | | ODP2VOUT2 | 0x00 |
| 46H | ODP 2 State 3 Output Voltage | | | | | | | | ODP2VOUT3 | 0x00 |
| 47H | ODP 2 State 4 Output Voltage | | | | | | | | ODP2VOUT4 | 0x00 |
| 48H | ODP 2 Timeout 0 [7:0] | | | | | | | | ODP2TOUT0_0 | 0x00 |
| 49H | ODP 2 Timeout 0 [15:8] | | | | | | | | ODP2TOUT0_1 | 0x00 |
| 4AH | ODP 2 Timeout 0 [23:16] | | | | | | | | ODP2TOUT0_2 | 0x00 |
| 4BH | ODP 2 Timeout 1 [7:0] | | | | | | | | ODP2TOUT1_0 | 0x00 |
| 4CH | ODP 2 Timeout 1 [15:8] | | | | | | | | ODP2TOUT1_1 | 0x00 |
| 4DH | ODP 2 Timeout 1 [23:16] | | | | | | | | ODP2TOUT1_2 | 0x00 |
| 4EH | ODP 2 Timeout 2 [7:0] | | | | | | | | ODP2TOUT2_0 | 0x00 |
| 4FH | ODP 2 Timeout 2 [15:8] | | | | | | | | ODP2TOUT2_1 | 0x00 |
| 50H | ODP 2 Timeout 2 [23:16] | | | | | | | | ODP2TOUT2_2 | 0x00 |
| 51H | ODP 2 Timeout 3 [7:0] | | | | | | | | ODP2TOUT3_0 | 0x00 |
| 52H | ODP 2 Timeout 3 [15:8] | | | | | | | | ODP2TOUT3_1 | 0x00 |
| 53H | ODP 2 Timeout 3 [23:16] | | | | | | | | ODP2TOUT3_2 | 0x00 |
| 54H | Prescale | | | | ODP 2 Rising Slew Rate 0 | | | | ODP2SLEWUP0 | 0x00 |
| 55H | Prescale | | | | ODP 2 Rising Slew Rate 1 | | | | ODP2SLEWUP1 | |
| 56H | Prescale | | | | ODP 2 Rising Slew Rate 2 | | | | ODP2SLEWUP2 | |
| 57H | Prescale | | | | ODP 2 Rising Slew Rate 3 | | | | ODP2SLEWUP3 | |
| 58H | Prescale | | | | ODP 2 Falling Slew Rate 0 | | | | ODP2SLEWDOWN0 | |
| 59H | Prescale | | | | ODP 2 Falling Slew Rate 1 | | | | ODP2SLEWDOWN1 | |
| 5AH | Prescale | | | | ODP 2 Falling Slew Rate 2 | | | | ODP2SLEWDOWN2 | |
| 5BH | Prescale | | | | ODP 2 Falling Slew Rate 3 | | | | ODP2SLEWDOWN3 | |
| 5CH | Regulator 1 PGOOD Blank Time | | | | | | | | ODP1PGBLANK | 0x00 |
| 5DH | ODP 1 Input Select 1 | | | | ODP 1 Input Select 0 | | | | ODP1ACT0 | 0xFF |
| 5EH | Reserved | | | | ODP 1 Input Select 2 | | | | ODP1ACT1 | 0x0F |
| 5FH-FFH | RESERVED | | | | | | | | RESERVED | |

## 8 Packaging

All dimensions are in millimeters unless otherwise noted.




| DIMENSION (mm) | | | |
|---|---|---|---|
| SYMBOL | MIN | NOM | MAX |
| A | 0.8000 | 0.850 | 0.9000 |
| A3 | | 0.200 | |
| b | 0.180 | 0.250 | 0.300 |
| D | | 8.000 | |
| D2 | 6.500 | 6.650 | 6.800 |
| E | | 8.000 | |
| E2 | 6.500 | 6.650 | 6.800 |
| e | | 0.500 | |
| L | 0.350 | 0.400 | 0.450 |
| θ | 0 deg. | | 14 deg. |