PSG5220-EK

Evaluation Kit User's Guide

Advanced SATA Power Management Unit Evaluation Kit User's Guide

PSG5220

PSG5220 is a highly integrated power management IC with dual synchronous step-down PWM controllers for SATA drive power management in notebooks. Interfaces for monitoring activity, coupled with advanced On-Demand Power™ algorithms, enable the regulated output voltages of the integrated switching regulators to be adaptively scaled in correlation with actual power demand. The real-time tracking of supply voltage to activity enables maximum power savings by minimizing the power spent on maintaining worst-case headroom in power distribution.

PSG5210

PSG5210 is a highly integrated power management IC with a synchronous step-down PWM controller for SATA drive power management in notebooks. Interfaces for monitoring activity, coupled with advanced On-Demand Power™ algorithms, enable the regulated output voltage of the integrated switching regulator to be adaptively scaled in correlation with actual power demand. The real-time tracking of supply voltage to activity enables maximum power savings by minimizing the power spent on maintaining worst-case headroom in power distribution.

Evaluation Kit (PSG5220-EK)

The advanced SATA power management unit evaluation kit is a single board module (pictured below in Figure 1) for the evaluation and integration of the PSG5220 and PSG5210 into designs. The evaluation kit includes the PSG5220 IC and a bill of materials for required operation.

This document describes the evaluation kit for the PSG5220 and also the PSG5210. Specific design information and electrical specifications regarding the IC itself can be found in the PSG5220 / PSG5210 datasheets.

Applications

- Laptop Computers
- Ultra-Mobile PCs
- Portable Media Players
- Other Mobile Devices

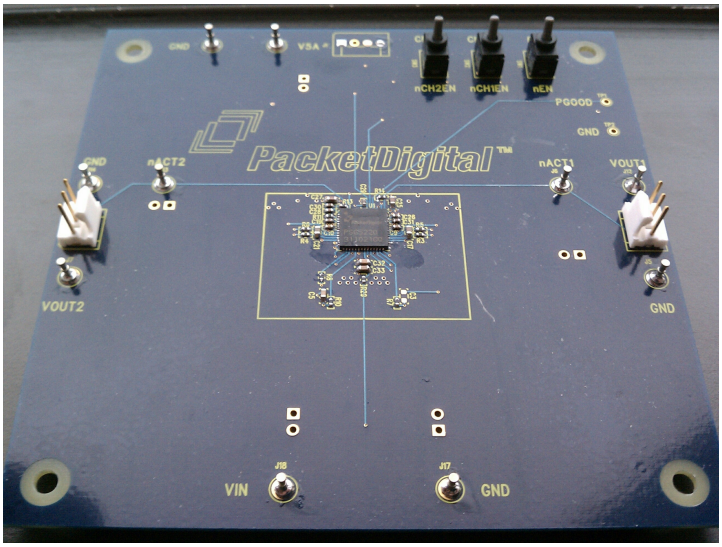

Figure 1: PSG5220 Evaluation Board

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1 Objective/Scope

This document is the user's guide for the implementation of PSG220 or PSG5210 into designs. It utilizes the PSG5220-EK evaluation kit from Packet Digital. The evaluation kit includes the PSG5220 IC and a bill of materials for required operation.

2 Reference Documents

Please contact Packet Digital for any of the following documents:

- PSG5220 Datasheet
- PSG5210 Datasheet
- PSG5220-EK Evaluation Kit Datasheet
- PSG52x0 Validation Plan

3 Introduction to PSG52X0 Power Management IC Family

3.1 PSG5220

PSG5220 is a highly integrated power management IC with dual synchronous step-down PWM controllers for SATA drive power management in notebook computers. Interfaces for monitoring activity, coupled with advanced On-Demand Power™ algorithms, enable the regulated output voltages of the integrated switching regulators to be adaptively scaled in correlation with actual power demand. The real-time tracking of supply voltage to activity enables maximum power savings by minimizing the power spent on maintaining worst-case headroom in power distribution. PSG5220 is a constant-on-time voltage regulator.

PSG5220 is ideal for notebook products with both optical and hard disk drives. One output channel of the PSG5220 can be configured for On-Demand Power™ operation of the ODD and the other for the HDD.

3.2 PSG5210

PSG5210 is a highly integrated power management IC with a synchronous step-down PWM controller for SATA drive power management in notebook computers. Interfaces for monitoring activity, coupled with advanced On-Demand Power™ algorithms, enable the regulated output voltage of the integrated switching regulator to be adaptively scaled in correlation with actual power demand. The real-time tracking of supply voltage to activity enables maximum power savings by minimizing the power spent on maintaining worst-case headroom in power distribution. PSG5210 is a constant-on-time voltage regulator.

PSG5210 is ideal for notebook and netbook products with only a hard disk drive, only a solid state drive or any other mobile application requiring a single output channel.

4 PSG5220 Demonstration Kit

The advanced SATA power management unit evaluation kit is a single board module for the evaluation and integration of the PSG5220 into designs. The evaluation kit includes the PSG5220 IC and a bill of materials for required operation.

4.1 Electrical Specifications

The following table provides electrical specifications for external connections to the demonstration kit. Complete electrical specifications for the PSG5220 and PSG5210 IC are listed in their respective datasheet.

Table 1: PSG5220-EK Electrical Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{VIN}	Input Voltage Range, VIN	External Voltage applied to VIN	6.5		24	V
V_{V50}	Input Voltage Range, V50	External Voltage applied to V50	4.5	5	5	V
I_{OUT}	Maximum Output Current: V_{O1} and V_{O2}		3			A

5 Configuration and Equipment

Below are the contents of the PSG5220 Demonstration Kit, the recommended test equipment and how to configure all of this.

5.1 PSG5220 Demonstration Kit Contents

- PSG5220-EK Printed Circuit Board (see Figure 1 on page 1)
- SATA power adapter board
- 7 pin SATA data cable
- 3 pin SATA power/ground/activity cable
- SMBUS to USB converter

5.2 Recommended Test Equipment

The following test equipment is recommended to support the use of the evaluation kit and for the validation of PSG5220/PSG5210:

- Digital Sampling Oscilloscope
- Differential oscilloscope probes
- Multimeters
- Data acquisition hardware/software, ie National Instruments Labview
- Bench power supplies
- Packet Digital PowerSage graphical users interface
- SMBUS Master such as National Instruments USB-8451

5.3 Configuration

Three switches are provided for enabling PSG5220. EN/nEN is the global enable and all chip functions, including the SMBUS interface, are placed in a standby mode when switched to nEN. Volatile memory settings will be retained as long as power is supplied. Independent channel enables are provided through CH1EN/nCH1EN and CH2EN/nCH2EN.

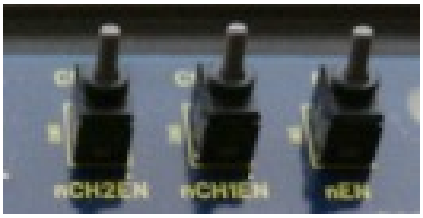

Figure 2: Channel Enable Switches

Surface-mount 2512 resistors have been placed on all power inputs and outputs. These are populated with zero-Ohm resistors but can be replaced with current sensing resistors for precise power measurements. Jumpers are available in parallel with these sense resistor locations for easy connection to differential test equipment.

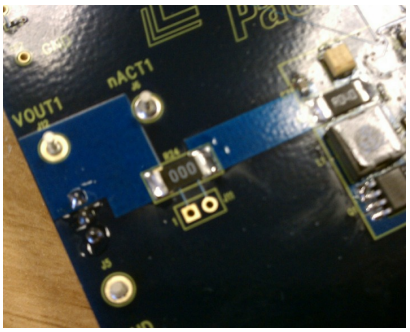

Figure 3: Current Sense Resistor

PSG5220 is highly configurable through SMBUS programmable settings. These settings configure output voltage, transition times, and On-Demand Power™ operation. See section 8 for more information on manually configuring output voltage through SMBUS.

6 Test Setup and Results

6.1 Test Setup

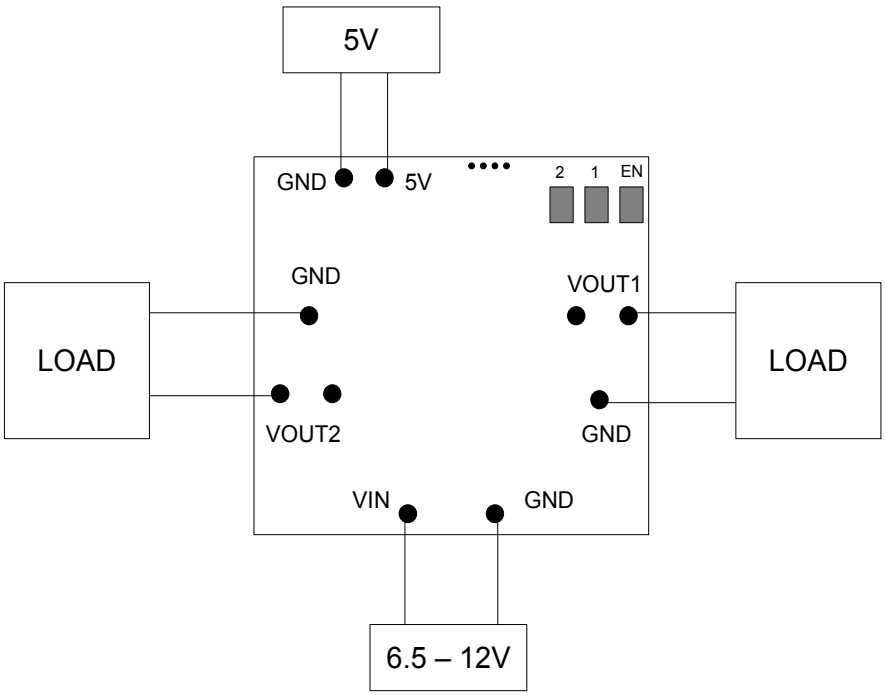

Figure 4: Evaluation Kit External Connections for PSG5220.

6.2 Test Procedure

- Set Switches to the following settings: nEN, nCH1EN, and nCH2EN
  - PSG5210: set only nEN, nCH1EN
- Connect Power Supplies for VIN (6.5V – 12V), V50 (5V), grounds, and test equipment where appropriate.
- Apply VIN/GND and V50/GND.
- Switch nEN to EN to enable the device.
- Communicate over SMBUS, if required. Please see PSG5220 / PSG5210 datasheets and PSG52X0 Validation plan for more information on SMBUS.
- For PSG5220, switch nCH1EN and/or nCH2EN to CH1EN and/or CH2EN. This will start-up the respective regulator channel.
  - For PSG5210, switch nCH1EN to CH1EN.
- Verify the voltage on Vout1 (and/or Vout2 if PSG5220) is at 5v.
- Perform required tests or validation procedure. Note, recommended tests are included in the PSG52X0 Validation plan.

6.3 Observed Test Results

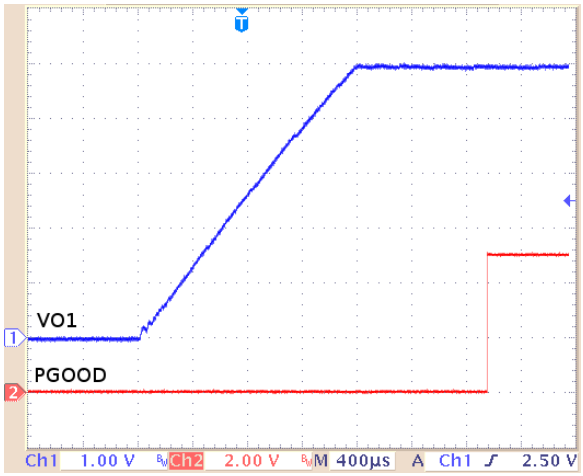

Figure 5: Start-up Sequence

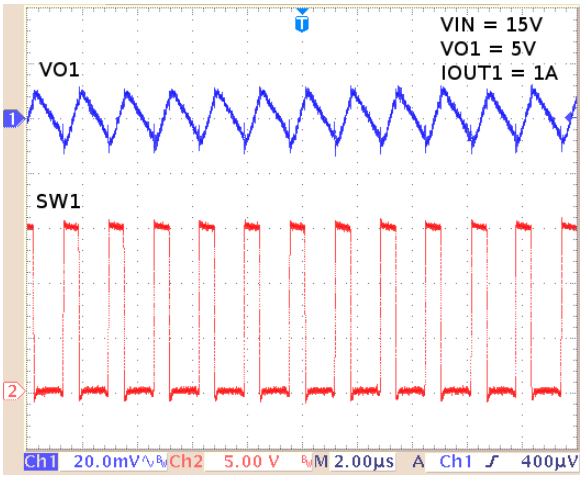

Figure 6: Output Voltage Ripple, CCM operation

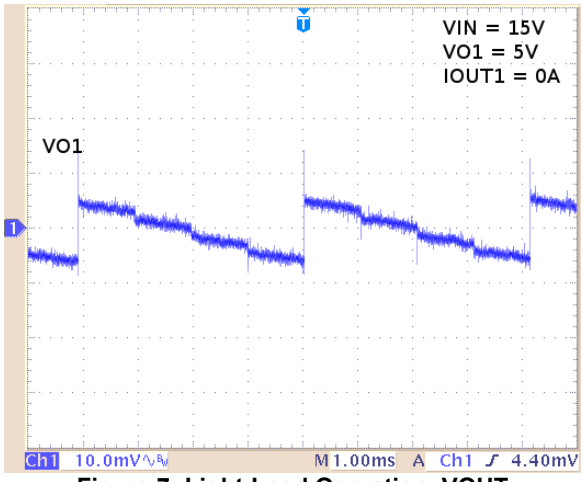

Figure 7: Light-Load Operation, VOUT

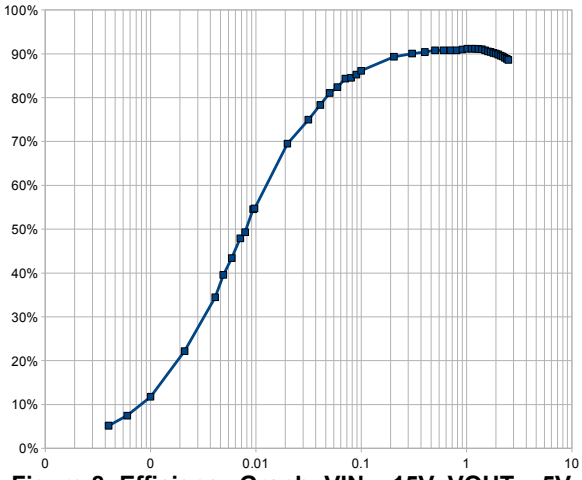

Figure 8: Efficiency Graph; VIN = 15V, VOUT = 5V

7 SMBUS Communication

The PSG5220 serial interface is compatible with the SMBUS 2.0 specification. SMBCLK is the serial clock input and SMBDAT is the bidirectional serial data. PSG5220 is configured as a slave on the SMBUS and has a fixed 7-bit slave address of 0x61. PSG5220 supports 'read byte', 'write byte', and 'block write' as described by the SMBUS specification.

The complete register maps for PSG5220/PSG5210 are in their respective datasheet.

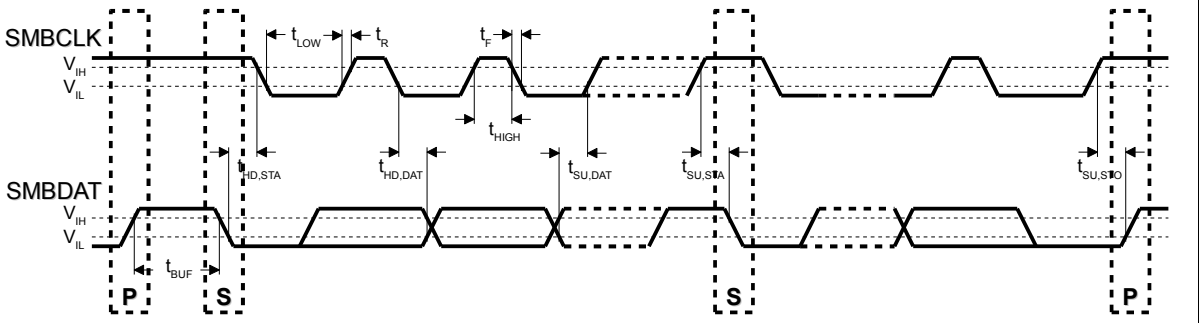

Figure 9: Timing Diagram for SMBUS Communication

Table 2: SMBUS Timing Parameters

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMB}	SMBus clock frequency		10		100	kHz
t_{LOW}	SMBus clock low time	Measured from $V_{IL(MAX)}$ to $V_{IL(MAX)}$	4.7			µs
t_{HIGH}	SMBus clock high time	Measure from $V_{IH(MIN)}$ to $V_{IH(MIN)}$	4.0			µs
$t_{r,SMB}$	SMBus rise time				1	µs
$t_{f,SMB}$	SMBus fall time				0.3	µs
t_{OF}	Output fall time	C_L = 400 pF, I_O = 3mA,			250	ns
$t_{TIMEOUT}$	SMBDAT and SMBCLK time low for reset of SMBus		25		35	ms
$t_{SU,DAT}$	Data setup time		250			ns
$t_{HD,DAT}$	Data hold time		300			ns
$t_{HD,STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated.		4			µs
$t_{SU,STO}$	Stop condition setup time		4			µs
$t_{SU,STA}$	Repeated start condition setup time		4.7			µs
t_{BUF}	Bus free time between stop and start conditions		4.7			µs

Procedure

- Run Test Procedure from section 6.2 on page 8.
- You will need to connect SMBUS master equipment as described in the Validation Plan.
- Read register 0x03 (result: 0x08) to verify regulator is enabled. For PSG5220 only, validate the second channel by reading register 0x22 (result: 0x08) to verify regulator is enabled.

The procedure above verifies that external connections to SMBUS are correct.

8 Manual Output Voltage Configuration

When On-Demand Power™ is not enabled, the PSG5220/PSG5210 operates as a static-output voltage regulator. The output voltage can be manually adjusted using the SMBUS serial interface through the registers ODP1VMAN, ODP2VMAN, or VMAN. PSG5220 uses ODP1VMAN and ODP2VMAN for output channels 1 and 2, respectively. VMAN is the register used for the single output channel in PSG5210.

Table 3 lists the register settings for ODP1VMAN, ODP2VMAN, and VMAN that correspond to manual output voltages. The output voltage will change immediately when the SMBUS write is complete.

Table 3: Manual Output Voltage Register Settings

Register Code	Vout
0x00	5.0V
0x08	4.9V
0x11	4.8V
0x19	4.7V
0x22	4.6V
0x2A	4.5V
0x33	4.4V
0x3b	4.3V
0x44	4.2V
0x4C	4.1V
0x55	4.0V

9 On-Demand Power™

On-Demand Power™ (ODP) describes the operation of PSG5220/PSG5210 delivering only the amount of power needed at the time that it's needed, based on activity being monitored. Refer to the PSG5220/PSG5210 datasheets for more detail.

Register settings are required for On-Demand Power™ operation. Contact Packet Digital engineering support for On-Demand Power™ Register settings for your specific HDD or ODD if needed.

After your specific On-Demand Power™ registers have been written, On-Demand Power™ can be enabled. For both PSG5220 and PSG5210, the following register enables On-Demand Power™ for power savings on channel 1:

Table 4: Enable ODP for Energy Savings (Channel 1)

Address		Data
0x03		
	HDD	0x09
	ODD	0x0D

For PSG5220 only, the following register enables On-Demand Power™ for power savings on channel 2:

Table 5: Enable ODP for Energy Savings (Channel 2)

Address		Data
0x22		
	HDD	0x09
	ODD	0x0D

10 Graphical User Interface

Packet Digital's graphical user interface (GUI) allows for easy access to internal register settings. Utilizing a USB connection with a PC, On-Demand Power settings and manual voltage outputs can be modified without the need of a SMBUS master or command line interface. Figure 10 shows a snapshot of the GUI.

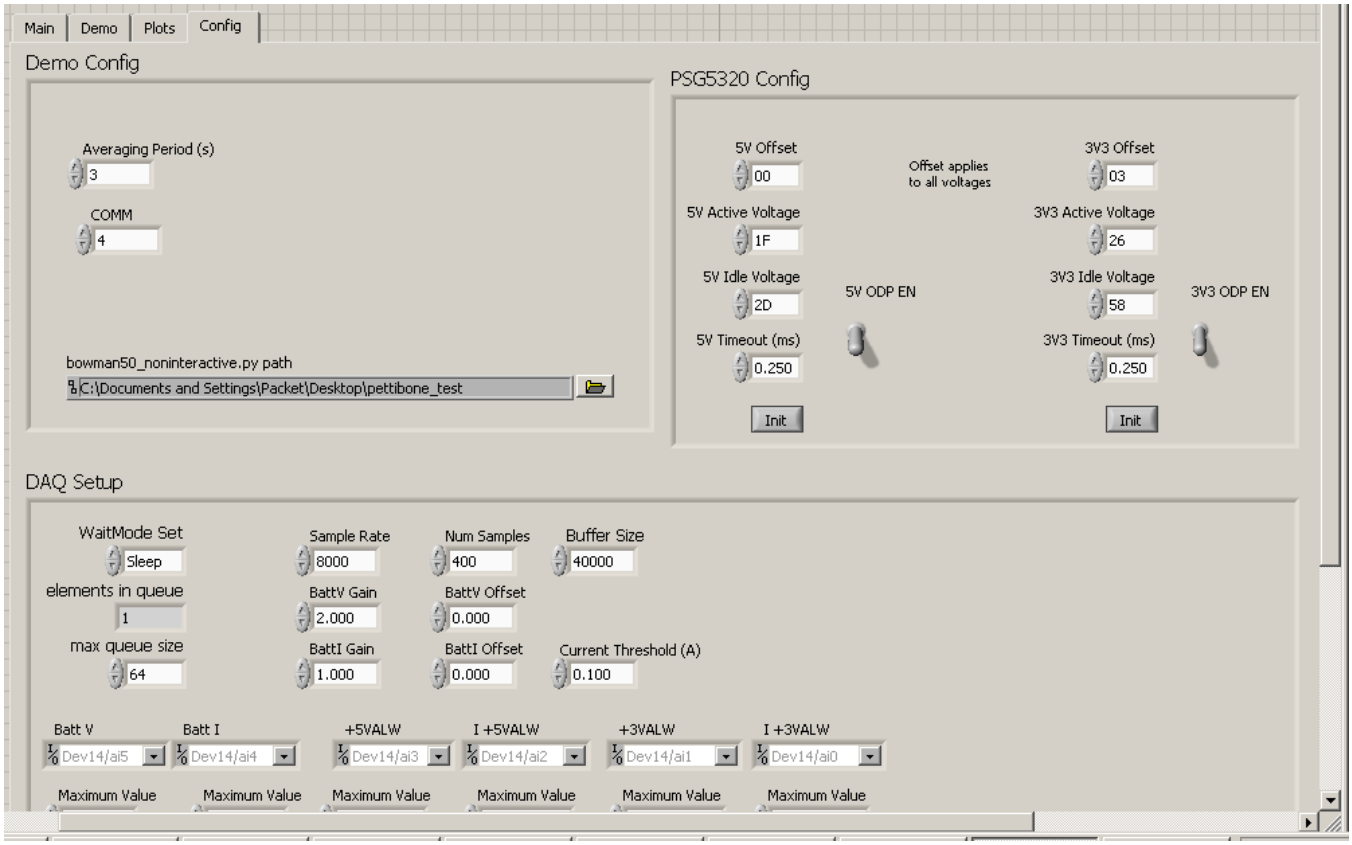

Figure 10: Graphical User Interface

The GUI supports communication through the USB interface to the PowerSage™ PSG5220/PSG5210 evaluation kit with the included SMBUS to USB converter. Settings that control algorithms for On-Demand Power™ (ODP) voltage levels, timeouts, thresholds, and inputs can be adjusted through this interface.

10.1 Voltage Control

Active and idle voltages can be set by their corresponding 8-bit hexadecimal code with 0x00 corresponding to 5V and 0x55 corresponding to 4V. Hexadecimal codes are approximately linear between and beyond these points.

10.2 Timeout

State transition timeouts can be defined for the ODP algorithm. Input as milliseconds, the GUI converts automatically to the corresponding register setting.

10.3 Threshold

Current thresholds are used by On-Demand Power™ to determine real-time power usage. Modifying the current threshold value adjusts how ODP reacts to changing load currents.

10.4 On-Demand Power Enable

A toggle switch is available to enable and disable On-Demand Power™. When disabled, the voltage regulator resumes default 5V operation.

10.5 Init

The Init button in the GUI commits settings from the user input fields to the PSG5220 through the USB interface.

11 Schematic

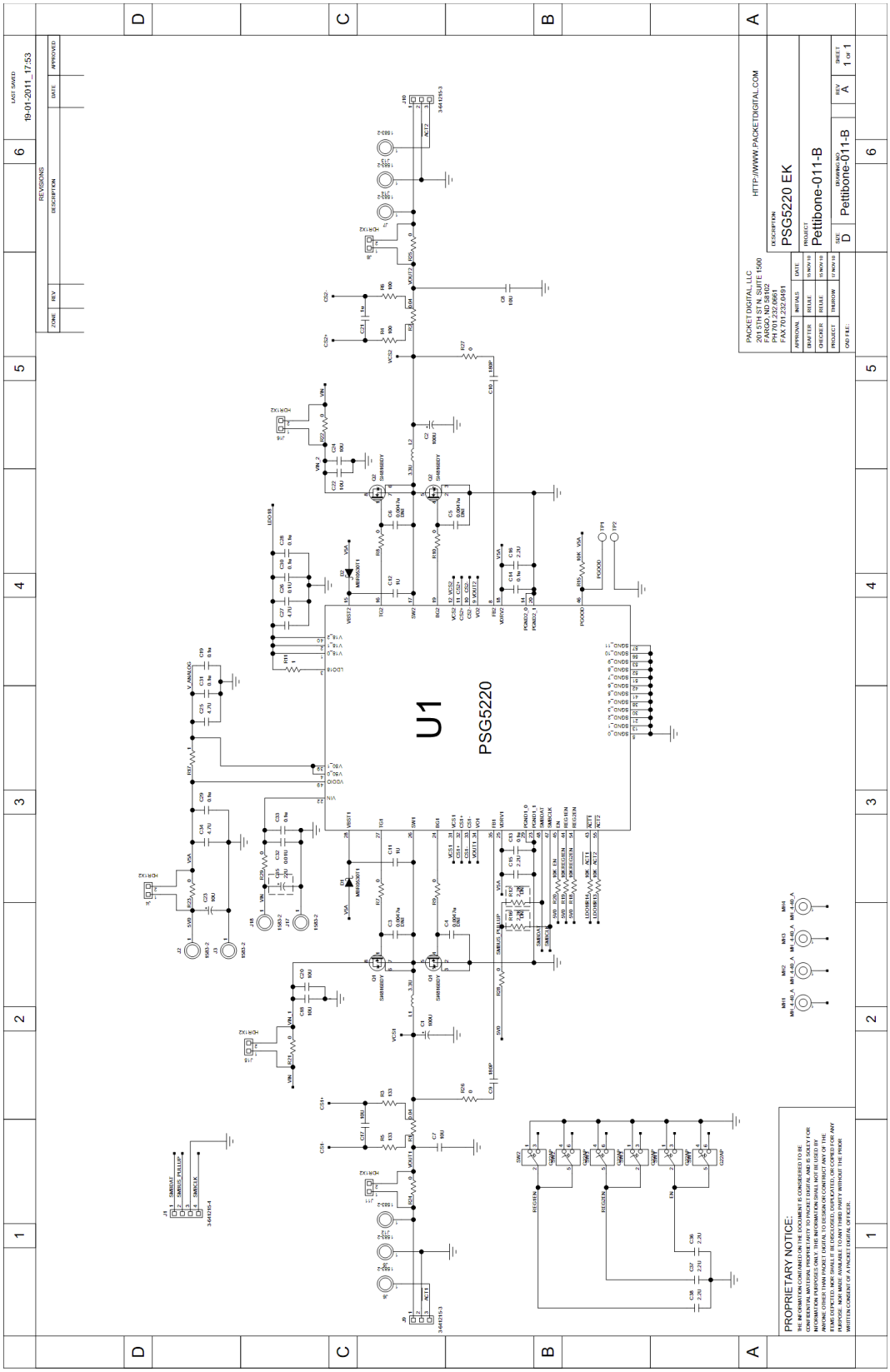

Figure 11: PSG5220-EK Schematic

12 Bill of Materials

Table 6: PSG5220 BOM

Reference-Designators	Description	Footprint	Manufacturer	Part Number	QTY
U1	PowerSage PSG5220	QFN-56	Packet Digital	PSG5220	1
C1-2	100µF Capacitor, Tantalum, 6.3V	3528-21	Kemet	T520B107M006ATE015	2
C11-12, C21	1 µF Capacitor, Ceramic, 50V	603	Taiyo Yuden	UMK107BJ105KA-T	3
C13-14, C19, C26, C28-C31	0.1µF Capacitor, Ceramic	402	Panasonic	ECJ-0EB1C104K	8
C15-16, C36-38	2.2 µF Capacitor, Ceramic	603	Panasonic	ECJ-1VB1A225K	5
C18, C20, C22, C24	10µF Capacitor, Ceramic, 35V	1210	Kemet	C1210C106M6PACTU	4
C23	10µF Capacitor, Tantalum, 35V	7343-31	Kemet	T491D106M035AT	1
C25, C27, C34	4.7µF Capacitor, Ceramic	603	TDK Corporation	C1608X5R1A475K	3
C32	10000pF Capacitor, Ceramic 50V	603	Panasonic	ECJ-1VB1H103K	1
C33	0.1µF Capacitor, Ceramic 50V	603	Murata	GRM188R71H104KA93D	1
C35	22µF Capacitor, Tantalum, 35V	7343-31	Kemet	T495D226K035ATE300	1
C7-8, C17	10µF Capacitor, Ceramic	603	Panasonic	ECJ-1VB0J106M	3
C9, C10	180pF Capacitor, Ceramic, 50V	402	Panasonic	ECJ-0EC1H181J	2
D1-2	Diode, Schottky, 30V, 0.5A	SOD-123	On Semiconductor	MBR0530T1G	2
J1	Connector, 4 Pos, 100 mil	3-641215-4	Tyco Electronics	3-641215-4	1
J2-3, J5-7, J12-14, J17-18	Turret	1502-2	Keystone Electronics	1502-2	10
J9-10	Connector, 3 Pos, 100 mil	3-641215-3	Tyco Electronics	3-641215-3	2
L1-2	3.3µH SMD	XPL7030	Coilcraft	XPL7030-332ML_	2
Q1-2	Dual NMOS, Schottky	SOIC-8	Vishay	SI4816BDY-T1-E3	2
R1	0.04Ω Resistor. 3W, 1%	2512	Bourns	CRA2512-FZ-R040ELF	1
R11,R17	1Ω Resistor	402	Panasonic	ERJ-2GEJ1R0X	2
R12,R16	2.2kΩ Resistor	402	Panasonic	ERJ-2GEJ222X	2
R13-15, R18-R20	10kΩ Resistor	402	Yageo	RC0402FR-0710KL	6
R2	0.08Ω Resistor. 3W, 1%	2512	Bourns	CRA2512-FZ-R080ELF	1
R21-25	0.0Ω Resistor	2512	SEI	RMCF 1 0 R	5
R3, R5	133Ω Resistor	402	Panasonic	ERJ-2RKF1330X	2
R4, R6	100Ω Resistor	402	Panasonic	ERJ-2GEJ101X	2
R7-10, R26-29	0.0Ω Resistor	402	Panasonic	ERJ-2GE0R00X	8
SW1-3	DPDT Swtich	G22	NKK	G22AP	3

Important Notice:

This Evaluation/Demonstration Board and kit is intended for engineering development, demonstrations, and evaluation purposes.

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