APPLICATION NOTE

ANP135 | The SEPIC with coupled and uncoupled inductors

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01. INTRODUCTION AND THEORETICAL BACKGROUND

The Single-Ended-Primary-Inductor-Converter, popularly known as SEPIC, is a non-isolated, switching power supply topology generating an output voltage that can be higher or lower than the input voltage. This is a common requirement in battery-powered applications as well as those with fluctuating input and/or output voltages, like photovoltaic converters (PV), automotive electronics, offline LED lighting and battery chargers, amongst others.

The SEPIC power stage (Figure 1) is built with two inductors (L_1 and L_2), two capacitors (C_{AC} and C_{out}), a main control transistor (Q_1) and a complementary switch which can be a transistor (Q_2) or a diode (D_1), there drawn as simple switches to highlight their function. Note how its input stage resembles that of a boost converter, resulting in a continuous input current which eases EMI filtering requirements. Its output stage is similar to that of a buck-boost converter, resulting in a discontinuous, pulsating current. However, unlike a standard buck-boost topology, the input and output voltages in the SEPIC have the same polarity, which is an important advantage in many applications. Both input and output stages are linked by the AC-coupling capacitor (C_{AC}).

The particular operation of the SEPIC allows L_1 and L_2 to share the same magnetic core and be built as a coupled-inductor instead of two separate power inductors. This approach not only reduces the component count, but also requires less inductance for the same AC ripple current on each winding. Furthermore, magnetically coupling the windings allows implementing ripple current steering, a technique that helps to lower EMI filtering requirements. In addition, and contrary to the usual case, a high leakage inductance can actually be advantageous in the SEPIC, as will be shown.

In this application note, the SEPIC in continuous as well as discontinuous conduction modes of operation (CCM and DCM) is analyzed, including formulae and important design guidance. The ripple current steering technique and the important role of leakage inductance are also studied. Analytical results are supported by SPICE simulations and measurements on a real DC-DC SEPIC converter prototype.

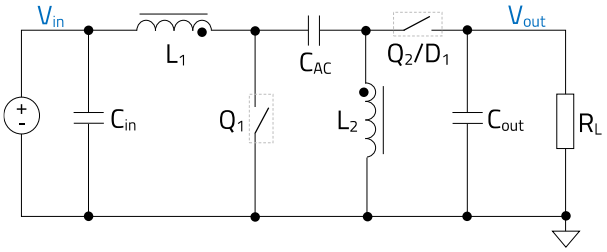

Figure 1: SEPIC power stage

02. PRINCIPLE OF OPERATION

2.1 The AC-coupling capacitor (C_{AC})

The SEPIC is a PWM-controlled converter, where the duty-cycle of the control transistor (Q_1), and indirectly its conduction time (Δt_{on}), regulates the amount of energy transferred from the input to the output stage and load.

The energy is transferred via the capacitor C_{AC}, which AC-couples the input and output stages, while blocking any DC-current between them, thus providing inherent short-circuit protection of the output. When Q_1 is not switching but just held open, L_1 and L_2 can be simplified to their winding resistances (R_{L1} and R_{L2}), and since DC current cannot flow, the DC input voltage appears entirely across C_{AC}, irrespective of Q_2/D_1 state (Figure 2). In normal operation, Q_1 is switching and an AC displacement current will flow through C_{AC}, with its amplitude directly proportional to C_{AC} value.

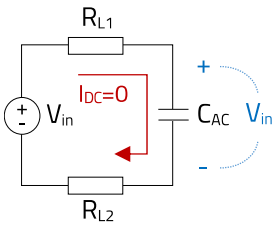

Figure 2: Equivalent circuit with Q1 held open (no switching)

Figure 3 shows the same SEPIC circuit as in Figure 1 but with both inductors magnetically coupled. Is this not actually a flyback converter? Well, it depends, especially on how the impedance of C_{AC} at the switching frequency ($Z_{Cac}(f_{sw})$) compares to the impedance of the leakage inductance (L_K) of the coupled inductor ($Z_{Lk}(f_{sw})$) (resistive elements included).

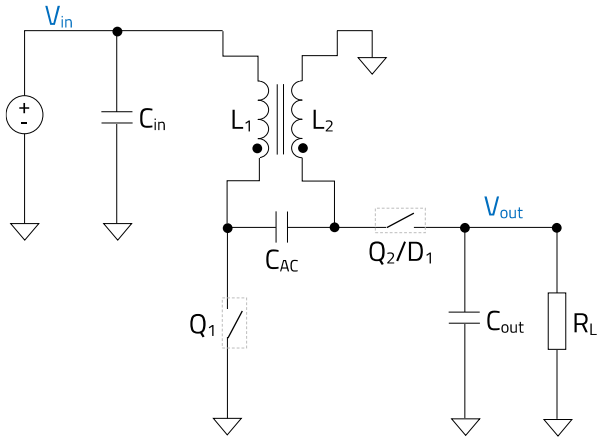

Figure 3: The role of C_{AC}: A SEPIC or a Flyback ?

If C_{AC} is small enough so that its impedance at the switching frequency is very high, only a negligible AC displacement current will be able to flow from the primary (input) to the secondary (output) side. In such a case, C_{AC} will just add to the total primary-to-secondary parasitic capacitance of the coupled power inductor, without affecting the converter's functionality, which will operate as a flyback. The energy will be transferred from input to output via the magnetic field coupling L_1 and L_2, and not via C_{AC}.

Conversely, if C_{AC} is high enough to appear almost as a short-circuit at the switching frequency, the energy will be transferred via C_{AC} instead, and the circuit in Figure 3 will operate as a SEPIC. In this case, a small AC ripple will be superimposed on the DC input voltage across C_{AC}. Note that, unlike in a flyback, in the SEPIC the magnetic coupling of L_1 and L_2 is not meant for energy transfer between the input and output stages.

If, when using two separate power inductors, the value of C_{AC} is too low, with its resulting high impedance at the switching frequency, it will simply decouple and in turn disconnect the input and output stages. Energy cannot be transferred and the converter will simply not function.

An approximate minimum value of C_{AC} for proper functioning of a CCM-SEPIC with separate inductors is as below:

$$C_{AC} > \frac{V_{out} \cdot I_{out} \cdot (1 - D) \cdot T_{sw}}{0.1 \cdot (V_{in})^2} \qquad (E.1)$$

In E.1, 'D' is the duty-cycle of the PWM signal controlling the conduction time of Q_1, and 'T_{sw}' the switching period.

In a worst-case scenario, E.1 would rarely yield a value below the two-digit 'nF' range. However, the minimum required AC-coupling capacitance will be much higher when using a coupled inductor, especially one with a high coupling factor. Such a case will be studied in later section 4.3.

2.2 Operation on a full switching cycle

Figure 4 shows the equivalent circuit of a SEPIC during the on-time of the control transistor Q_1 (Δt_{on}). Here, Q_2/D_1 is open, current through L_1 builds up and the inductor stores energy from the source and input capacitor. L_2 also stores energy during Δt_{on}, delivered in this case by C_{AC}, while the load current is supplied by the output capacitor. Note how L_1 and L_2 both see the input voltage applied across them during Q_1 on-time.

During the off-time of Q_1 (Δt_{off}) (Figure 5), Q_2/D_1 conducts and both inductors L_1 and L_2 now release the energy stored during Δt_{on}. Part of this energy is used to recharge C_{AC} and C_{out} and the rest supplies the load. Note how the voltage across C_{AC} opposes that of the input source, and as a result, the voltage across the inductors during Δt_{off} corresponds to the output voltage of the converter, plus the small voltage drop across Q_2/D_1, ignored in this simplified analysis.

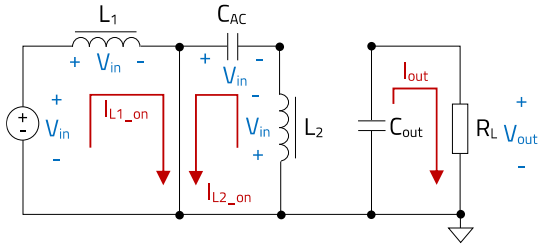

Figure 4: Equivalent circuit during the on-time of Q_1 (Δt_{on})

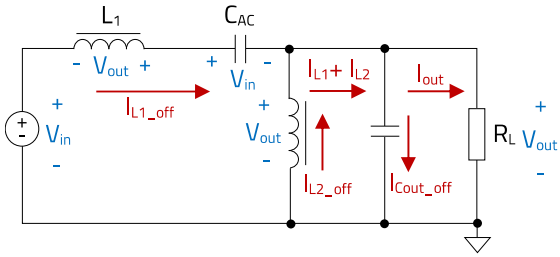

Figure 5: Equivalent circuit during the off-time of Q_1 (Δt_{off})

In steady-state operation, the average volt-second product across any inductors in a full switching period must be zero. This can be expressed as:

$$V_{L(on)} \cdot \Delta t_{on} + V_{L(off)} \cdot \Delta t_{off} = 0 \qquad (E.2)$$

Where $V_{L(on)}$ and $V_{L(off)}$ are the average voltages across the inductors during Δt_{on} and Δt_{off}, respectively. E.2 also shows why the polarity of $V_{L(on)}$ and $V_{L(off)}$ during Δt_{on} must be opposite to that during Δt_{off}, as observed in Figure 4 and Figure 5.

The on and off times of Q_1 are:

$$\Delta t_{on} = D \cdot T_{sw} \qquad (E.3)$$

$$\Delta t_{off} = (1 - D) \cdot T_{sw} \qquad (E.4)$$

03. CIRCUIT ANALYSIS

In the previous analysis from Figure 4 and Figure 5, it was considered that the current through the inductors was constantly changing during the entire switching period (i.e. increasing during Δt_{on} and decreasing during Δt_{off}). This is known as continuous-conduction-mode operation (CCM). However, as the load current decreases, the converter will eventually enter discontinuous-conduction-mode operation (DCM), which in the SEPIC, is characterized by the current through the inductors becoming constant (and thus their voltage becoming zero) during a part of Δt_{off}.

Based on this, in a CCM-SEPIC, E.2 can be expressed as:

$$V_{in} \cdot \Delta t_{on} = V_{out} \cdot \Delta t_{off} \qquad \text{(E.5)}$$

However, for a DCM-SEPIC, $V_{L(off)} \neq V_{out}$ and E.5 is not valid. Therefore, the operation of the converter will be studied separately for CCM and DCM. The schematic of Figure 6 will be used as reference for all plotted and measured waveforms in this document, observing the convention of voltage polarity and positive current direction shown. The analysis will be performed considering separate power inductors first, while the implications of magnetically coupling the inductors will be covered in section 4, building upon these results.

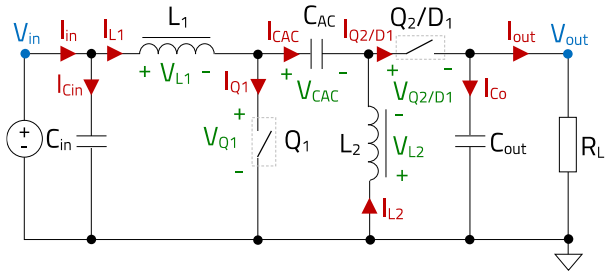

Figure 6: SEPIC reference schematic for current/voltage polarities

3.1 Continuous Conduction Mode (CCM)

From E.3, E.4 and E.5, the ideal voltage conversion ratio of the SEPIC in CCM is obtained:

$$A_{v_CCM} = \frac{V_{out}}{V_{in}} = \frac{D}{1 - D} \qquad \text{(E.6)}$$

E.6 represents a non-linear relationship between the input and output voltages, as plotted in Figure 7. Observe how the converter steps up the input voltage for a duty cycle above 50%, while it steps it down for a duty cycle below 50%.

So far, ideal components without parasitic resistances were considered. But in a real converter, these resistive elements will actually cause the duty cycle to (slightly) deviate from the ideal value obtained in E.6.

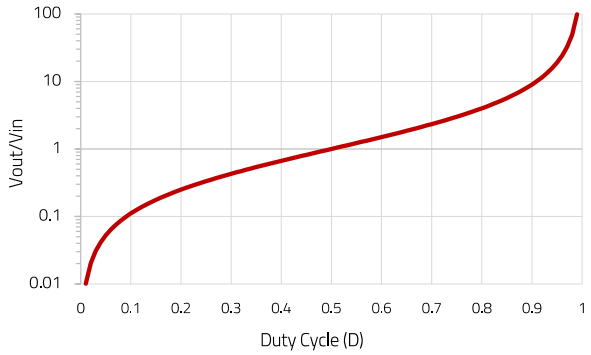

Figure 7: Ideal voltage conversion ratio of SEPIC

Examples of such elements are the winding resistances of L_1 and L_2, the ESR of C_{AC} and the conduction resistances of Q_1 and Q_2 (in case of using a transistor instead of a diode (D_1)).

Although the output voltage level can be easily brought down to zero by just holding Q_1 open, the expression in E.6 suggests that V_{out} would increase without bounds as the duty-cycle approaches '1' (i.e. 100%). However, in reality the voltage gain will reach a finite maximum level, with a further increase of the duty cycle causing a reduction of the output voltage instead, which will finally collapse to zero for D=100%. The maximum attainable voltage conversion ratio depends on components' resistive elements and the converter load (R_L).

The real voltage gain of the CCM-SEPIC when factoring in the influence of resistive elements like L_1 winding resistance (R_{L1}) as well as the conduction resistances of Q_1 (R_{Q1}) and Q_2 (R_{Q2}) is given in E.7. Observe how the ideal voltage conversion ratio from E.6 is now multiplied by a factor which will be lower than '1', and whose exact value will depend on how the respective ohmic losses compare to the load resistance. For a set load (R_L), higher values of resistive elements result in a lower maximum attainable voltage gain.

$$A_V = \frac{D}{1-D} \cdot \frac{1}{\left(1 + \frac{D}{(1-D)^2} \cdot \frac{R_{L1}}{R_L} + \frac{D^2}{(1-D)^2} \cdot \frac{R_{Q1}}{R_L} + \frac{D}{1-D} \cdot \frac{R_{Q2}}{R_L}\right)} \qquad \text{(E.7)}$$

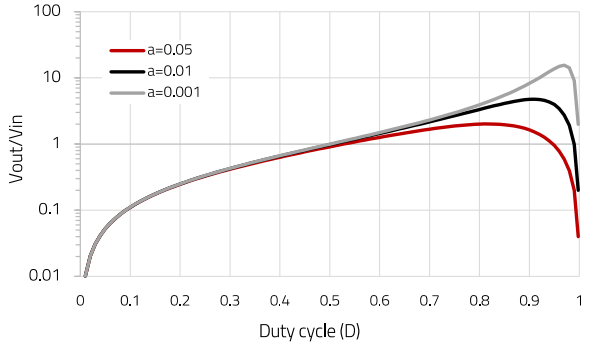

Figure 8: Real voltage conversion ratio of SEPIC for a=R_{L1}/R_L

In E.7, the resistive elements are weighted based on their conduction time during a switching period, and with all resistive elements being equal, R_{L1} would be the dominant factor, followed by R_{Q1}.

In Figure 8, the expression from E.7 is plotted considering three different ratios of $a=R_{L1}/R_L$. For a set R_L, a higher R_{L1} limits the maximum step-up conversion ratio, and the same applies for R_{Q1} and R_{Q2}. Note that additional resistive elements like the ESR of C_{AC} and to a much lesser extent the DCR of L_2 will also have an impact but their contribution was not shown in E.7. Although this scenario rarely happens, it is important to be aware of this limitation when using the SEPIC in applications with very wide V_{in} or V_{out} and/or high load current.

Waveforms, formulae and measurements in CCM

Figure 9 shows the main ideal waveforms of the CCM-SEPIC. Formulae for calculation of component values as well as estimation of voltage and currents are provided here, accompanied by experimental results on a SEPIC converter prototype operating at the following conditions and with the main passive power stage components as below:

V_{in} = 18 V

V_{out} = 12 V

I_{out} = 2 A

f_{sw} = 200 kHz

L_1 - L_2: WE-PD 1050 7447714470 (47 µH, 80 mΩ)

C_{in} : WCAP-CSGP 885012209071 (2.2 µF, 10 mΩ)
(~ 2 µF with DC-bias)

C_{AC} : WCAP-CSGP 885012214005 (10 µF, 2.7 mΩ)
(~ 8.8 µF with DC-bias)

C_{out} : 2 x WCAP-CSGP 885012214005 (20 µF, 1.3 mΩ)
(~ 17.5 µF with DC-bias)

Regarding the semiconductor devices, Q_1 is an N-MOSFET (NVMFS5C682NL (Onsemi)), and D_1 a Schottky barrier diode (VSSA3L6S (Vishay)) on all results in this document.

For more details about the prototype board used, see A.1.

Inductors (L=L_1=L_2) calculations and results in CCM

As with other switching converters, the inductance value (L) is selected to limit the ripple current amplitude (ΔI_L) across the respective inductor. The inductors in the SEPIC (L_1 and L_2) operate independently, each of them storing and then delivering part of the energy that the load requires in a switching cycle.

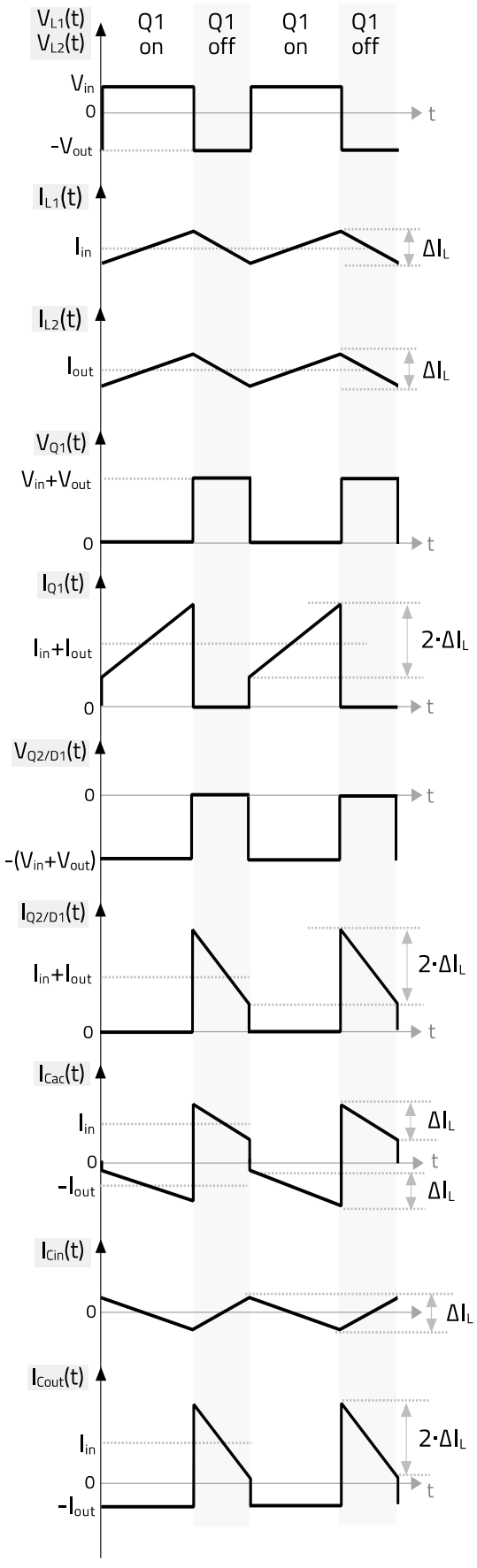

Figure 9: Main circuit waveforms of CCM SEPIC

This means that they could be selected of different inductance values if desired. However, in the vast majority of applications the same inductor part (L_1=L_2=L) is used to reduce cost thanks to a higher order volume. This will also be the case considered here.

E.8 is used to calculate the required inductance (L) based on the target inductor ripple current (ΔI_{L_CCM}).

$$L = \frac{V_{in} \cdot D}{f_{sw} \cdot \Delta I_{L_CCM}} = \frac{V_{in} \cdot D}{f_{sw} \cdot r \cdot I_{L_max}} \quad (E.8)$$

The ripple can be set as a factor of the maximum inductor DC current ($\Delta I_{L_CCM} = r \cdot I_{L_max}$), where 'r' is set between 0.2 and 0.4 and I_{L_max} will correspond to whichever is higher: the maximum average current through L_1 or through L_2 , given as I_{L1_max} and I_{L2_max}, respectively.

The average current through L_1 corresponds to the converter input DC current, obtained as below:

$$I_{L1} = I_{in} = \frac{V_{out} \cdot I_{out}}{\eta \cdot V_{in}} \quad (E.9)$$

In E.9, the parameter 'η' is the power efficiency of the converter at full load, which for most SEPIC designs is typically found between 0.85 and 0.92, with 0.9 being a good approximation for the initial calculation.

The inductor L_2 is part of the output stage of the converter, and its average current corresponds to the load current:

$$I_{L2} = I_{out} \quad (E.10)$$

The design approach followed here consists of using I_{L1_max} in E.8 if a step-up voltage conversion dominates ($I_{in_max} > I_{out_max}$), and conversely, using I_{L2_max} for a dominating step-down conversion.

The RMS currents through L_1 and L_2 are as below:

$$I_{L1_RMS} = \sqrt{I_{in}^2 + \frac{(\Delta I_L)^2}{12}} \approx I_{in} \quad (E.11)$$

$$I_{L2_RMS} = \sqrt{I_{out}^2 + \frac{(\Delta I_L)^2}{12}} \approx I_{out} \quad (E.12)$$

Experimental results for the previous specification are shown in Figure 10. From E.6, D=0.4 is calculated. To set the inductor ripple at around 40% of the output current of 2 A (i.e. to 0.8 A) at Vin=18 V, E.8 suggests L1=L2=L=45 µH. With the selected 47 µH, a ripple current amplitude of $\Delta I_{L1} = \Delta I_{L2} \approx 0.77$ A is calculated.

Oscilloscope channels 2 (green) and 3 (blue) show the currents through L_1 and L_2, respectively.

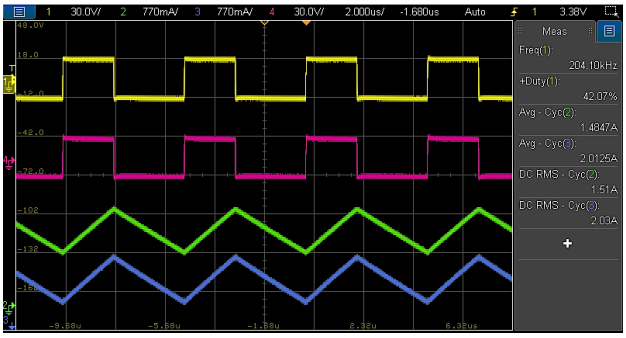

Figure 10: Measured L_1, L_2 CCM waveforms (I_{L1} (I), V_{L1} (I), I_{L2} (I), V_{L2} (I))

With both set to 770 mA per division, it can be directly seen how the measured ripple current agrees with calculation, while the measured average and RMS currents are practically the same, as already advanced.

The DC-current through L_1 (the input current) is around 1.48 A, which for this specification corresponds to an efficiency over 90 % (E.9). Observe how the voltage across the inductors is the same (channel-1 (yellow) for L_1 and channel-4 (magenta) for L_2, both on a 30 V/div scale). The values on the Y-axis correspond to channel-1, showing how the voltage is 18 V during the on-time, and 12 V during the off-time, equal to the input and output voltages of the converter. The measured duty-cycle is 0.415, slightly higher than the calculated value of 0.4. They closely agree thanks to the very low forward voltage drop across the output diode and the small effect of resistive elements, not accounted for in E.6.

For worst-case analysis, the maximum inductor ripple current happens at the maximum input voltage, whereas the maximum RMS currents occur when the SEPIC operates at the minimum input voltage and maximum load current.

Q_1 calculations and results in CCM

As observed in Figure 9, the control transistor Q_1 blocks a voltage during its off-time (Δt_{off}) which is the sum of the input and output voltages:

$$V_{Q1_off} = V_{in} + V_{out} \quad (E.13)$$

The RMS current through Q_1 is:

$$I_{Q1_RMS} = \sqrt{D \cdot \left((I_{in}+I_{out})^2 + \frac{(\Delta I_L)^2}{3} \right)} \approx (I_{in}+I_{out}) \cdot \sqrt{D} \quad (E.14)$$

In this design, Q_1 is implemented as an n-type MOSFET transistor. For the specification considered, calculated values of voltage and RMS currents are 30 V and 2.22 A. They agree with experimental results of Figure 11, showing Q_1 voltage (V_{Q1}) in channel-1 (yellow, 20 V/div) and Q_1 current (I_{Q1}) in channel-2 (green, 2 A/div).

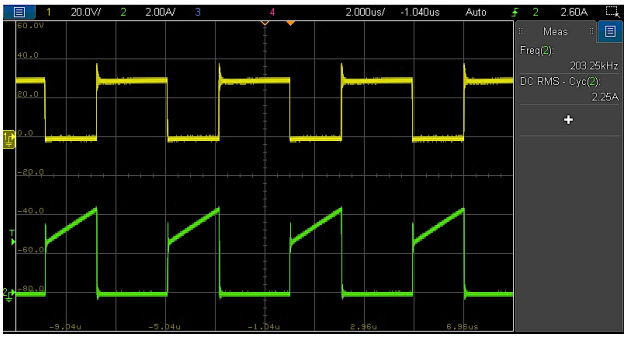

Figure 11: Measured Q_1 waveforms of CCM-SEPIC (V_{Q1} (), I_{Q1} ())

Note a current spike happening on Q_1 at the turn-on transition, causing a voltage overshoot with some ringing in the voltage waveform. This is caused by the charging of the parasitic capacitances existing between each of the two switching nodes of the SEPIC (i.e. nodes across C_{AC}) and circuit reference GND. To keep its amplitude and ringing low, the copper area of the switch nodes must be minimized, the same as the parasitic inductance and thus the area of the current loop formed by Q_1, C_{AC}, Q_2/D_1 and C_{out}.

Furthermore, selecting Q_1 and D_1 with very low output and junction capacitances, respectively, also helps in this endeavor, amongst other solutions not detailed here.

For worst-case considerations, the maximum voltage across drain-source of Q_1 happens at the maximum input and output voltages, whereas the maximum current amplitude and RMS level occur at minimum input voltage and full load.

Q_2/D_1 calculations and results in CCM

During its off-time, the voltage across Q_2/D_1 is the same as for Q_1:

$$V_{Q2/D1_off} = V_{in} + V_{out} \quad \text{(E.15)}$$

The RMS current of Q_2 is calculated as:

$$I_{Q2/D1_RMS} = \sqrt{(1 - D) \cdot \left((I_{in} + I_{out})^2 + \frac{(\Delta I_L)^2}{3} \right)} \quad \text{(E.16)}$$

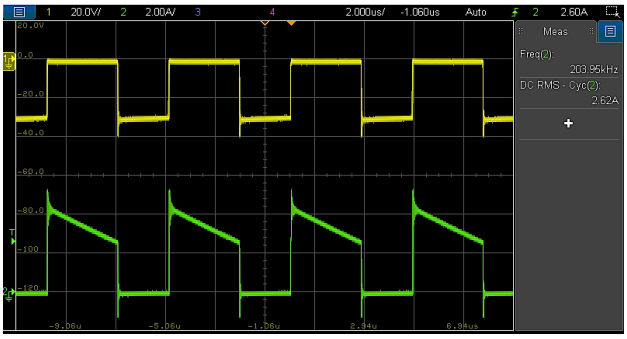

Figure 12: Measured Q_2/D_1 waveforms of CCM-SEPIC ($V_{Q2/D1}$ (), $I_{Q2/D1}$ ())

In our example, calculated values from E.15 and E.16 are 30 V and 2.7 A, respectively, in close agreement with measured results of Figure 12. In this case, the scales as well as voltage and current channels are the same as for Q_1. Observe the current spike on Q_2 at the turn-off transition, coinciding with Q_1 turn-on. With the diode used rated at 60 V blocking voltage, an RC snubber (100 Ω, 100 pF) was required across the diode to damp the voltage ringing and limit its negative undershoot to -40 V, well within ratings.

Worst-case operating conditions for Q_2/D_1 are the same as for Q_1, this is, maximum input and output voltages for blocking voltage rating (plus any overshoot) and minimum input voltage and full-load for highest RMS current.

C_{AC} calculations and results in CCM

For a set operating point, the voltage ripple across C_{AC} is approximated as follows (considering negligible ESR and ignoring the effect of the inductor AC ripple):

$$\Delta V_{CAC} = \frac{I_{in} \cdot (1 - D)}{f_{sw} \cdot C_{AC}} \quad \text{(E.17)}$$

When the ESR is considered (R_{CAC}), the voltage ripple across C_{AC} can be approximated as below:

$$\Delta V_{Cac_ESR} \approx \frac{I_{in} \cdot (1 - D)}{f_{sw} \cdot C_{AC}} + R_{CAC} \cdot (I_{in} + I_{out} + \Delta I_L) \quad \text{(E.18)}$$

Note that the voltage ripple caused by the ESR and that generated by the capacitance are phase shifted 90° from each other, thus the exact ripple amplitude will be lower, but E.18 is a good starting point.

As seen in Figure 9, the capacitor C_{AC} sustains a high RMS displacement current, which can be estimated as below:

$$I_{Cac_RMS} = \sqrt{(1-D) \cdot (I_{L1_RMS})^2 + D \cdot (I_{L2_RMS})^2} \quad \text{(E.19)}$$

With the effective 8.8 µF, 2.7 mΩ part selected, the calculated RMS current and ripple voltage values are 1.72 A and 500 mV (using E.17). Measurement results are shown in Figure 13 (V_{Cac} on channel-1 (yellow, 500 mV/div) and I_{Cac} on channel-2 (green, 2 A/div)), where a ripple voltage slightly over 500 mV is observed, not far from the estimation, while the measured RMS current is 1.73 A, matching well the theoretical value.

For worst-case analysis, both maximum RMS current and ripple voltage occur when operating at minimum input voltage and full load.

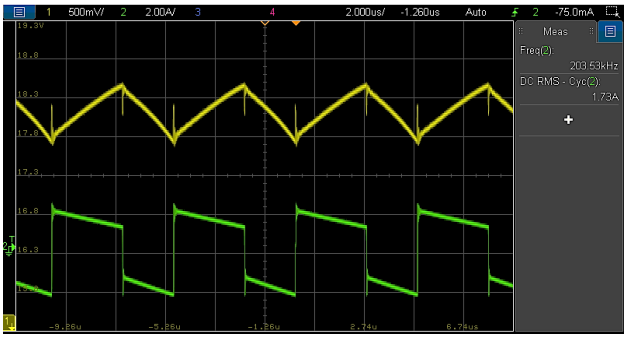

Figure 13: Measured C_{AC} waveforms of CCM-SEPIC (V_{Cac} (), I_{Cac} ())

C_{in} calculations and results in CCM

The input capacitance is set to limit the converter input voltage ripple as follows (neglecting ESR):

$$C_{in} = \frac{\Delta I_L}{8 \cdot f_{sw} \cdot \Delta V_{in}} \quad \text{(E.20)}$$

If the impedance of the input capacitor at the switching frequency ($Z_{Cin}(f_{sw})$) is higher than its ESR (R_{Cin}), then the expression in E.20 is used. Conversely, if it is lower, then the capacitive contribution is neglected and the input voltage ripple is approximated as below:

$$\Delta V_{R_{Cin}} \approx R_{Cin} \cdot \Delta I_L \quad \text{(E.21)}$$

The RMS current through the input capacitor is:

$$I_{C_{in_RMS}} = \frac{\Delta I_L}{2 \cdot \sqrt{3}} \quad \text{(E.22)}$$

E.22 shows that C_{in} sustains a much lower RMS current than C_{AC} or C_{out}, thus requiring much less capacitance for the same ripple amplitude.

With the effective 2 µF, 10 mΩ part selected, the calculated RMS current and ripple voltage values at the operating point considered are 0.23 A and 240 mV (using E.20). Measurements are shown in Figure 14 (V_{Cin} on channel-1 (yellow, 200 mV/div) and I_{Cin} on channel-2 (green, 770 mA/div)). Observe how the current ripple amplitude agrees with that of the input inductor L_1 (770 mA, E.11), while the measured voltage ripple is close to the calculated value.

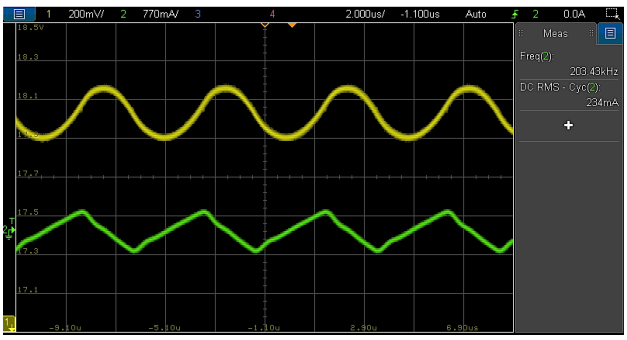

Figure 14: Measured C_{in} waveforms of CCM-SEPIC (V_{Cin} (), I_{Cin} ())

Worst-case maximum values for voltage and current happen at minimum input voltage, independent of load current.

C_{out} calculations and results in CCM

The output capacitance required to set the desired output voltage ripple (for negligible ESR) is as below:

$$C_{out} = \frac{I_{out} \cdot D \cdot T_{sw}}{\Delta V_{out}} \quad \text{(E.23)}$$

When considering its ESR (R_{Cout}), the output voltage ripple is approximated as:

$$\Delta V_{R_{Cout}} \approx R_{Cout} \cdot (I_{in} + I_{out} + \Delta I_L) \quad \text{(E.24)}$$

The displacement RMS current through the output capacitor is:

$$I_{Cout_RMS} = \sqrt{D \cdot (I_{out})^2 + (1 - D) \cdot \left(I_{in}^2 + \frac{(\Delta I_L)^2}{3} \right)} \quad \text{(E.25)}$$

With effective values of 17.5 µF and 1.3 mΩ as selected, calculated values for RMS current and voltage ripple for the example considered are 1.72 A and 230 mV, respectively. These are in line with experimental results of Figure 15 (V_{Cout} on channel-1 (yellow, 200 mV/div) and I_{Cout} on channel-2 (green, 2 A/div)).

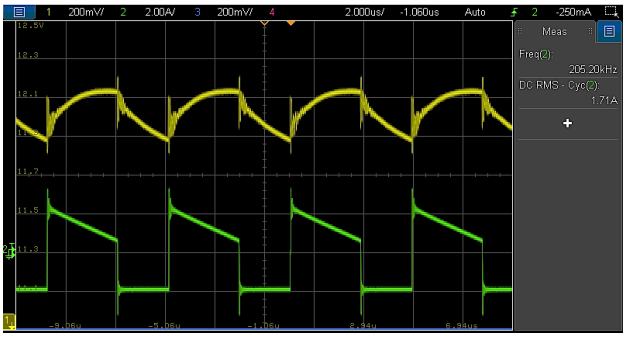

Figure 15: Measured C_{out} waveforms of CCM-SEPIC (V_{Cout} (), I_{Cout} ())

Observe the parasitic switching spikes followed by a short ringing on the switching transitions. This noise is affected by the parasitic inductance of the current loops through C_{out}, exacerbated in this case by the loop of wire used for the current probe measurement. Keeping a low output impedance over a wide frequency range helps to reduce the amplitude peaks of this noise on the output voltage rail and limit their negative effects on EMI. When required, this can be accomplished, for example, by paralleling several MLCC capacitors of the same value with a small package (for lower parasitic inductance), and/or using an additional well-damped low-pass LC filter at the output, amongst other solutions.

3.2 Boundary CCM-DCM

As the converter load current reduces, so do the average currents through L_1 and L_2, eventually reaching a level at which their sum equals the peak-to-peak ripple current amplitude. This condition represents the boundary between CCM and DCM operation in a SEPIC, as below:

$$I_{L1} + I_{L2} = \Delta I_L \qquad \text{(E.26)}$$

Based on the inductors' positive current direction shown in Figure 6, for a step-down voltage conversion ($V_{out}<V_{in}$), the current through L_1 will reverse direction during part of the switching period before the boundary CCM-DCM is reached. Conversely, for a step-up voltage conversion ($V_{out}>V_{in}$), the current through L_2 will reverse direction instead. This is the case shown in Figure 16.

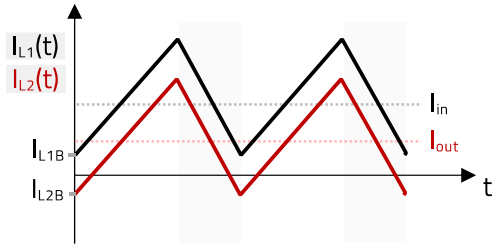

Figure 16: Boundary CCM-DCM of SEPIC for $V_{out} > V_{in}$

Alternatively, it can also be seen how the CCM-DCM transition point is reached when the minimum instantaneous currents across the inductors (at the beginning and end of a switching cycle) become equal but opposite ($I_{L1B} = -I_{L2B}$). This current level (I_{LB}) is calculated as below:

$$I_{L1B} = -I_{L2B} = I_{LB} = \frac{I_{OB}}{2} \cdot \left(\frac{V_{out}}{V_{in}} - 1\right) \qquad \text{(E.27)}$$

Note how in E.27, for $V_{out}>V_{in}$, I_{L1B} will be positive and I_{L2B} negative, whereas for $V_{out}<V_{in}$, I_{L1B} will be negative and I_{L2B} positive instead, signaling the inductor current direction. In E.27, I_{OB} is the load current at the boundary CCM-DCM (a.k.a. critical or boundary load current), calculated as follows:

$$I_{OB} \approx \frac{V_{in} \cdot D \cdot (1 - D)}{L \cdot f_{sw}} \qquad \text{(E.28)}$$

Considering the SEPIC specification of the previous example, the boundary load current at V_{in}=18 V (D≈0.41) is calculated from E.28 as I_{OB}≈0.47 A, whereas the minimum inductor current at the boundary (I_{LB}) is around 75 mA (E.27).

SPICE simulation results in Figure 17 and Figure 18, at I_{out}=0.47 A (Boundary CCM-DCM) and I_{out}=0.4 A (DCM) respectively, confirm the calculated transition point. L_1 current reverses direction in this case, as a voltage step down conversion is performed.

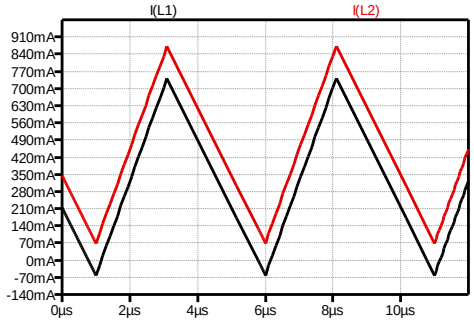

Figure 17: L_1, L_2 currents for I_{out}=0.47 A (CCM-Boundary) (LTspice™)

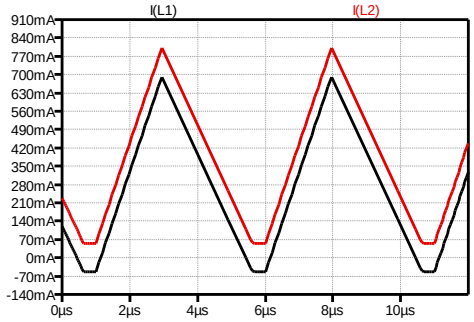

Figure 18: L_1, L_2 currents for I_{out}=0.4 A (DCM) (LTspice™)

At the transition point, the instantaneous minimum currents of L_1 and L_2 are 70 mA and of opposite direction, while a third time interval appears in DCM, during which the inductors' currents are not zero, but stay at a level different than that calculated in E.27.

3.3 Discontinuous Conduction Mode (DCM)

As the load current reduces below the critical level (I_{OB}), the current through the complementary switch (Q_2/D_1) will need to reverse direction. When using a bidirectional-current device like a MOSFET transistor for Q_2 this is not an issue, and the converter will keep operating in what is known as 'forced-continuous-conduction-mode' (FCCM). However, when a unidirectional-current device like a diode is used as the complementary switch (D_1) (Figure 19), current cannot reverse direction and the converter will operate in DCM for $I_{out}<I_{OB}$. This is also known as non-synchronous operation.

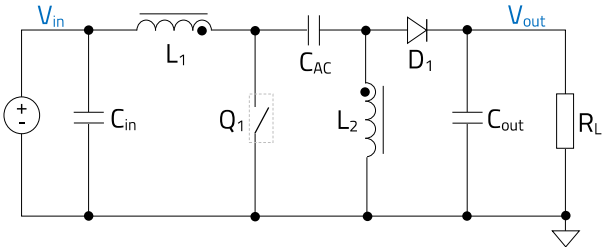

Figure 19: Non-synchronous SEPIC converter power stage

Contrary to the case of single-inductor converters, in the SEPIC both inductors L_1 and L_2 will still conduct current during

the entire switching period even in DCM operation as long as $V_{in} \neq V_{out}$, as advanced in the results of Figure 18.

Figure 20 shows the current waveforms of L_1 and L_2 in DCM for a voltage step-up conversion. Note how the switching cycle can be divided into three time intervals: Δt_1, Δt_2 and Δt_3. The first interval Δt_1 corresponds to Δt_{on}, the conduction time of Q_1, where the current through each winding builds up. The two remaining intervals (Δt_2 and Δt_3) correspond to the off-time of Q_1 (Δt_{off}). Here, the second interval Δt_2 is characterized by a decreasing current through each inductor as they deliver energy, while during the third interval, the inductors' currents remain constant at levels $I_{L1D}=I_{LD}$ and $I_{L2D}=-I_{LD}$, with I_{LD} calculated as:

$$I_{LD} = I_{L1D} = -I_{L2D} = \frac{V_{out}}{2 \cdot R_L} \cdot \left(\frac{V_{out}}{V_{in}} - 1 \right) \qquad \text{(E.29)}$$

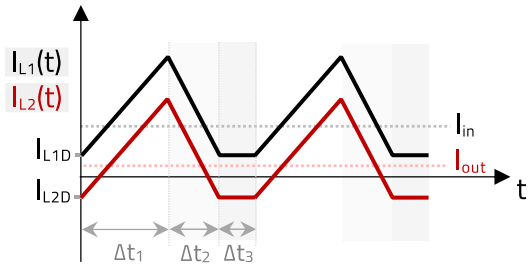

Figure 20: L_1 and L_2 currents of DCM SEPIC (example $V_{out} > V_{in}$)

Like in previous E.27, the sign of the result in E.29 indicates which inductor current will be negative and thus reverse direction during Δt_3 based on Figure 6 convention.

During Δt_3, as D_1 is reverse-biased and Q_1 in the off-state, the current I_{LD} flows in the loop formed by C_{in}, L_1, C_{AC} and L_2, as shown in Figure 21, which depicts the equivalent circuit during Δt_3 with the inductors replaced by their DCRs.

This circulating current I_{LD} causes some charge and thus energy exchange between C_{in} and C_{AC} capacitors. In a voltage step-up conversion, the current in the loop will flow clockwise (red dotted line), with C_{in} providing some charge to C_{AC}, while for a voltage step-down conversion, the current will flow counterclockwise (black dotted line), and it will be C_{AC} that provides some charge to C_{in}.

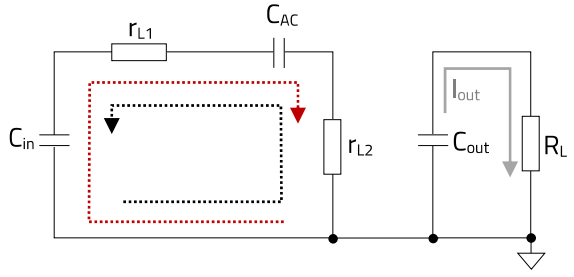

Figure 21: Loop current I_{LD} during Δt_3 in a DCM SEPIC

For $V_{in}=V_{out}$, the circulating current I_{LD} will be zero. In all cases, the output capacitor supplies the load during Δt_3.

Voltage Conversion in DCM

In DCM, as in CCM, the principle of inductor's volt-second balance over a full switching period in steady-state operation is used to obtain an analytical expression for the output voltage. However, in DCM only the time intervals Δt_1 and Δt_2 are relevant, as the inductors' voltage is zero during Δt_3. Then:

$$V_{in} \cdot \Delta t_1 = V_{out} \cdot \Delta t_2 \qquad \text{(E.30)}$$

In E.30, the time interval Δt_2 varies not only with 'D' and 'F_{sw}' (as in CCM), but also with load resistance (R_L) and inductance (L), as necessary to keep volt-second balance, as follows:

$$\Delta t_2 = \sqrt{\frac{L}{R_L \cdot f_{sw}}} \qquad \text{(E.31)}$$

Knowing that $\Delta t_1 = \Delta t_{on} = D/f_{sw}$, the voltage conversion in DCM is obtained from E.30 and E.31 as below:

$$A_{v_DCM} = \frac{V_{out}}{V_{in}} = D \cdot \sqrt{\frac{R_L}{L \cdot f_{sw}}} \qquad \text{(E.32)}$$

Once L and f_{sw} are fixed in the design, the duty-cycle will have to be adjusted as the load current varies in order to keep the output voltage at its target level, a task that a well-designed closed feedback loop will automatically do.

In Figure 22, the voltage conversion ratio of the DCM-SEPIC as a function of the duty-cycle is plotted for $L_1=L_2=10$ µH, $f_{sw}=200$ kHz and three different loads: $R_L=100$ Ω, 250 Ω and 1 kΩ, where the mentioned dependencies can be seen.

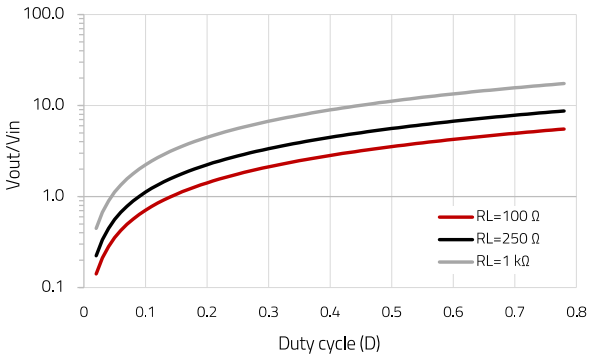

Figure 22: Voltage conversion ratio of DCM-SEPIC vs D (at R_L)

Waveforms, formulae and measurements in DCM

The ideal voltage and current waveforms of the DCM-SEPIC are shown in Figure 23 for a voltage step-up conversion (for a voltage step-down conversion the I_{LD} levels will just be the opposite as shown).

For the case of a SEPIC designed to operate exclusively in DCM, formulae to estimate components' ratings alongside experimental results are provided here.

The same SEPIC prototype board as in the CCM case is used, albeit with some changes in specification and components:

V_{in} = 18 V

V_{out} = 12 V

I_{out} = 0.7 A

f_{sw} = 200 kHz

L_1 & L_2 : WE-LHMI 7030 74437346100 (10 µH, 80 mΩ)

C_{in} & C_{AC}: WCAP-CSGP 885012214005 (10 µF, 2.7 mΩ)
(~ 8.8 µF with DC-bias)

C_{out} : 2 x WCAP-CSGP 885012214005 (20 µF, 1.3 mΩ)
(~ 17.5 µF with DC-bias)

Inductors (L_1 and L_2) calculations and results in DCM

Unlike CCM, in DCM the ripple current amplitude is higher than the average inductor current. The inductance $L=L_1=L_2$ is selected to set the maximum ripple current amplitude (ΔI_{L_max}) as follows:

$$L = \frac{V_{out} \cdot I_{out_max}}{\Delta I_{L_max}^2 \cdot f_{sw}} \quad \text{(E.33)}$$

For fixed V_{in} and V_{out}, the inductors' ripple current (ΔI_{L_DCM}) does not remain constant as in CCM, but reduces with load current (i.e. with higher R_L):

$$\Delta I_{L_DCM} = \frac{V_{out}}{\sqrt{L \cdot f_{sw} \cdot R_L}} \quad \text{(E.34)}$$

In DCM, the contribution of the AC ripple current amplitude to the RMS currents of L_1 and L_2 can no longer be neglected, and are obtained as below:

$$I_{L1_rms} = \sqrt{D \cdot \left(\frac{(\Delta I_L)^2}{3} + \Delta I_L \cdot I_{LD} \right) \left(1 + \frac{V_{in}}{V_{out}} \right) + I_{LD}^2} \quad \text{(E.35)}$$

$$I_{L2_rms} = \sqrt{D \cdot \left(\frac{(\Delta I_L)^2}{3} - \Delta I_L \cdot I_{LD} \right) \left(1 + \frac{V_{in}}{V_{out}} \right) + I_{LD}^2} \quad \text{(E.36)}$$

Where I_{LD} was defined in previous E.29.

For $L_1=L_2=L=10$ µH, and with a measured duty-cycle of 0.24, it is obtained from E.35 $\Delta I_L \approx 2.1$ A.

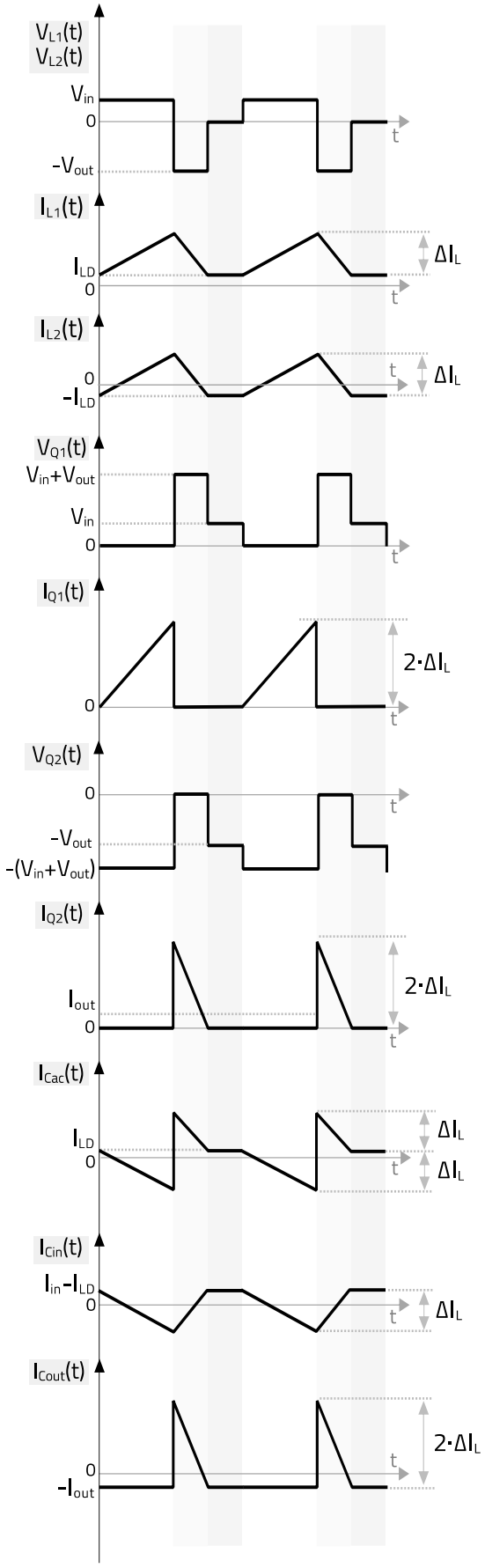

Figure 23: Ideal circuit waveforms of DCM SEPIC for $V_{out}>V_{in}$

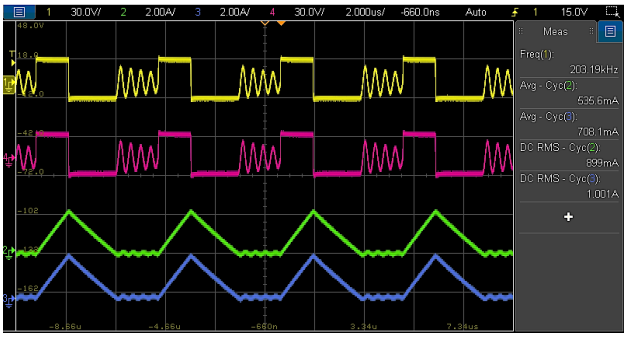

Figure 24: Measured L_1, L_2 waveforms of DCM-SEPIC (I_{L1} (I), V_{L1} (I), I_{L2} (I), V_{L2} (I))

Experimental measurements in Figure 24 show $I_{L1}=I_{in}\approx 0.54$ A, which corresponds to an efficiency of around 87 %. From E.29, it is obtained $I_{LD}=110$ mA and from E.35 and E.36, $I_{L1_RMS} \approx 0.9$ A and $I_{L2_RMS} \approx 1$ A.

Experimental results in Figure 24 show a close agreement with the calculations. Scale for voltages are 30 V/div while for inductor currents 2 A/div.

Observe how, during Δt_3, the average voltage across the inductors is zero but there is a large superimposed oscillation not shown in the ideal waveforms of Figure 23. This is typical of DCM operation and it is caused by the underdamped resonance of the inductors with the lumped parasitic capacitance appearing between the switching nodes of the SEPIC (both terminals across C_{AC}) and circuit reference ground. This parasitic capacitance is mainly affected by the output capacitance of Q_1 and the junction capacitance of D_1.

Observe how the oscillation frequency is much higher than the switching frequency. In this case, it is measured at 2.4 MHz, so its influence on EMI should be assessed. If problematic, it can be easily damped with an RC snubber at the expense of lower efficiency. In this case, a 1.5 nF capacitor and a 100 Ω resistor across Q_1 eliminate the oscillation, as shown in Figure 25. This incurs an efficiency penalty of around 2% at a load current of 0.7 A.

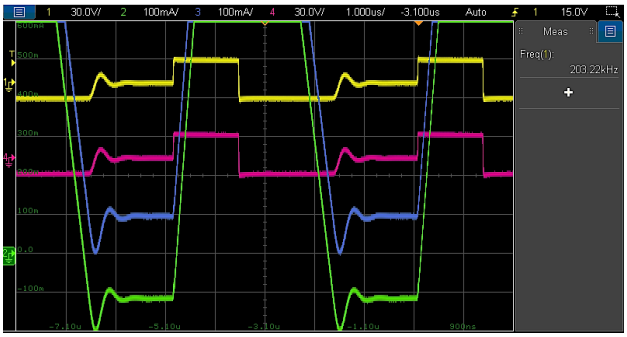

Figure 25: Measured L_1, L_2 waveforms of DCM-SEPIC with damped oscillation and zoomed I_{LD} detail (I_{L1} (I), V_{L1} (I), I_{L2} (I), V_{L2} (I))

Also in Figure 25, with the scale for the inductors currents set to 100 mA/div, an absolute level of I_{LD} around 100 mA is measured, in line with calculation. Note how the input current (green) reverses direction here, as a step-down conversion is being performed. Although I_{LD} is also included in the DCM equations shown in this section for completeness, in most cases its value is rather low compared to the ripple and average currents, and its influence can often be neglected, as in this example.

The rest of measurements shown here correspond to the original conditions of Figure 24 without the damping.

Q_1 calculations and results in DCM

As in CCM, in DCM Q_1 sees the sum of the input and output voltages across its terminals, this time during Δt_2:

$$V_{Q1_max} = V_{in} + V_{out} \qquad \text{(E.37)}$$

The RMS current through Q_1 in DCM is:

$$I_{Q1_RMS} = \sqrt{4 \cdot D \cdot \frac{(\Delta I_L)^2}{3}} \qquad \text{(E.38)}$$

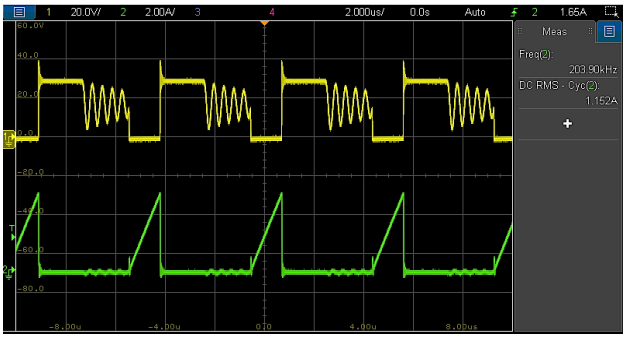

Figure 26: Measured Q_1 waveforms of DCM-SEPIC (V_{Q1} (I), I_{Q1} (I))

For the specification considered, calculated values of voltage and RMS currents are 30 V and 1.15 A, respectively. Experimental waveforms and measurements are shown in Figure 26, which are in agreement with calculated values.

D_1 calculations and results in DCM

The voltage across D_1 is the same as in CCM:

$$V_{Q2_max} = V_{in} + V_{out} \qquad \text{(E.39)}$$

The RMS current of D_1 in DCM is:

$$I_{Q2_RMS} = \sqrt{4 \cdot D \cdot \frac{V_{in}}{V_{out}} \cdot \frac{(\Delta I_L)^2}{3}} \qquad \text{(E.40)}$$

Values calculated in E.39 and E.40 are 30 V and 1.4 A, respectively, corresponding closely to the measured results of Figure 27.

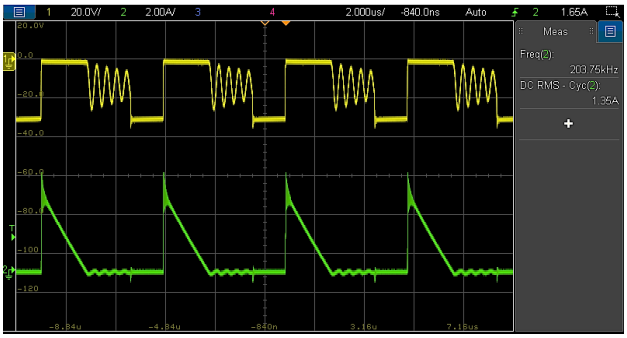

Figure 27: Measured D_1 waveforms of DCM-SEPIC (V_{D1} (), I_{D1} ())

C_{AC} calculations and results in DCM

The analytical expression to obtain the exact voltage ripple across C_{AC} in DCM is rather complex, even when neglecting its ESR. As a good starting point, C_{AC} can be set with E.41 and then further adjusted in simulation if necessary:

$$C_{AC} \sim \frac{1}{\Delta V_{AC} \cdot f_{sw}} \cdot \left(D \cdot \frac{V_{in}}{V_{out}} \cdot \left(\frac{\Delta I_L - I_{LD}}{2} \right) + (1 - D) \cdot I_{LD} \right) \quad \text{(E.41)}$$

The RMS current through C_{AC} is obtained as follows:

$$I_{Cac_rms} = \sqrt{D \cdot \left(\frac{(\Delta I_L)^2}{3} - \Delta I_L \cdot I_{LD} \right) + D \cdot \frac{V_{in}}{V_{out}} \cdot \left(\frac{(\Delta I_L)^2}{3} + \Delta I_L \cdot I_{LD} \right) + I_{LD}^2} \quad \text{(E.42)}$$

In Figure 28, an RMS current of 0.9 A is measured, matching the value calculated from E.42, while the measured ripple voltage is around 0.3 V for the selected capacitor (8.8 µF, 2.5 mΩ). For that ripple, the approximation in E.41 would suggest a capacitance of around 5 µF as a starting point.

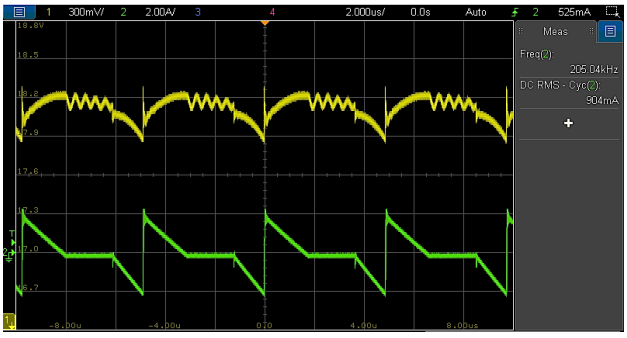

Figure 28: Measured C_{AC} waveforms of DCM-SEPIC (V_{Cac} (), I_{Cac} ())

C_{in} calculations and results in DCM

An approximation to set the input capacitance in DCM is given in E.43 (neglecting ESR):

$$C_{in} \approx \frac{(I_{in} - I_{LD}) \cdot (1 - D)}{\Delta V_{in} \cdot f_{sw}} \quad \text{(E.43)}$$

The RMS displacement current of the input capacitor is:

$$I_{Cin_rms} = \sqrt{D \cdot \left(1 + \frac{V_{in}}{V_{out}}\right) \cdot \left(\frac{(\Delta I_L)^2}{3} - \Delta I_L \cdot (I_{in} - I_{LD}) \right) + (I_{in} - I_{LD})^2} \quad \text{(E.44)}$$

Measurements are shown in Figure 29. Calculated RMS current is 0.68 A, in agreement with the experimental measurement. For 8.8 µF, the measured voltage ripple is around 0.2 V. Based on E.43 approximation, the capacitance required to set the same voltage ripple is around 12.5 µF.

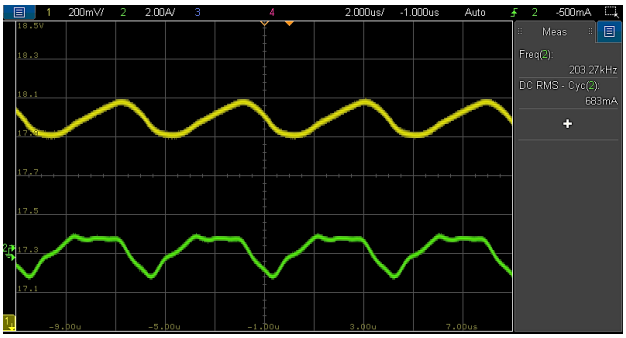

Figure 29: Measured C_{in} waveforms of DCM-SEPIC (V_{Cin} (), I_{Cin} ())

C_{out} calculations and results in DCM

The relationship between the output capacitance and the output voltage ripple in DCM is (for negligible ESR):

$$C_{out} \approx \frac{I_{out}}{\Delta V_{out} \cdot f_{sw}} \cdot \left(1 - D \cdot \frac{V_{in}}{V_{out}}\right) \quad \text{(E.45)}$$

The RMS displacement current for C_{out} is:

$$I_{Cout_rms} = \sqrt{2 \cdot D \cdot \frac{V_{in}}{V_{out}} \cdot \left(\frac{2 \cdot (\Delta I_L)^2}{3} - I_{out} \cdot \Delta I_L \right) + I_{out}^2} \quad \text{(E.46)}$$

The values of RMS current and ripple voltage calculated are 1.21 A and 130 mV, respectively, corresponding well to measurements of Figure 30. Ignoring the parasitic switching spikes, a voltage ripple of around 180 mV is observed, not far from the starting point approximation from E.45.

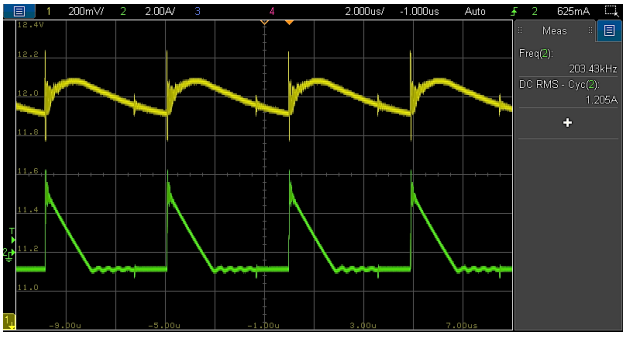

Figure 30: Measured C_{out} waveforms of DCM-SEPIC (V_{Cout} (), I_{Cout} ())

04. COUPLING THE WINDINGS

4.1 Ripple current amplitude: uncoupled vs. coupled

In the SEPIC, the voltage across each inductor at any instant in time is the same, forming the basis upon which the inductors' windings can share the same magnetic core.

The magnetic coupling of the inductors in a SEPIC can be represented as in the schematic of Figure 31, while previous Figure 3 also depicts an alternative arrangement for this. Here, the reference positive voltage polarities and current directions for each winding (L_1 and L_2) during Q_1 on-time (Δt_{on}) are shown.

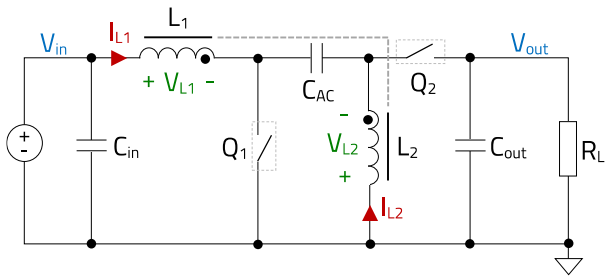

Figure 31: Schematic of SEPIC with magnetically coupled windings

It is essential to observe the windings' dotted terminal configuration, which follows the same convention as with transformers. They must be either both connected to C_{AC} (recommended) or to the DC nodes.

In the SEPIC, each inductor is driven by equal squarewave voltage waveforms in steady-state operation (ideal case). During Δt_{on}, the input voltage is applied across the inductor and the current rises with a 1st order slope, thus the common expression of voltage and current of an inductor in E.47 can be replaced by that of E.48, relating the inductor current ripple as a 1st order function of the constant volt-second applied across its self-inductance 'L' during Δt_{on}.

$$v_L(t) = L \cdot \frac{di_L(t)}{dt} \qquad \text{(E.47)}$$

$$V_{in} \cdot \Delta t_{on} = L \cdot \Delta i_L \qquad \text{(E.48)}$$

Based on Ampere's law, the current and, in turn, the generated magnetic flux ripple amplitudes are related as follows:

$$\Delta\Phi_{L_uncoupled} = \frac{L}{N} \cdot \Delta I_{L_uncoupled} \qquad \text{(E.49)}$$

Where 'N' is the winding's number of turns. From Faraday's law, the change of magnetic flux ($\Delta\Phi_L$) during Δt_{on} is related to the volt-second applied across the specific inductor winding as in E.50.

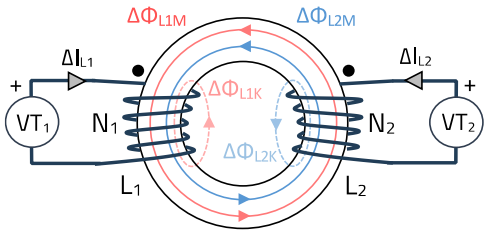

Figure 32: Volt-seconds-driven coupled inductor windings (ideal)

$$\Delta\Phi_{L_uncoupled} = \frac{V_{in} \cdot t_{on}}{N} \qquad \text{(E.50)}$$

In Figure 32, both inductors' windings are built on the same magnetic core (a toroid in this example). Consider the ideal case of both windings having the same number of turns 'N_1=N_2=N' and physical geometry, while being driven by equal volt-second sources (VT_1=VT_2=VT=V_{in}· Δt_{on}).

The winding polarity arrangement causes the magnetic flux generated in one winding to be in phase with that coupled from the other winding, effectively adding up in the core. Neglecting the leakage flux (i.e. $\Delta\Phi_{L1K}+\Delta\Phi_{L2K} << \Delta\Phi_{L1M}+\Delta\Phi_{L2M}$), the total magnetic flux enclosed by a winding is now composed of both: that generated by the winding itself plus that generated by the other winding:

$$\Delta\Phi_{L1_coupled} = \Delta\Phi_{L2_coupled} \approx \Delta\Phi_{L1M} + \Delta\Phi_{L2M} \qquad \text{(E.51)}$$

However, the same volt-second is still being applied across each winding as when they are uncoupled, so to satisfy E.50, the magnetic flux variation in the core for coupled windings needs to be the same as when they are uncoupled:

$$\Delta\Phi_{L1M} + \Delta\Phi_{L2M} = \Delta\Phi_{L_uncoupled} \qquad \text{(E.52)}$$

As both windings are identical in this example:

$$\Delta\Phi_{L1M} = \Delta\Phi_{L2M} = \frac{\Delta\Phi_{L_uncoupled}}{2} \qquad \text{(E.53)}$$

From E.49, the condition in E.53 is met when the coupled windings' ripple current is half that for the uncoupled case:

$$\Delta\Phi_{L1M} = \frac{L}{N} \cdot \frac{\Delta I_{L1_uncoupled}}{2} \qquad \text{(E.54)}$$

$$\Delta\Phi_{L2M} = \frac{L}{N} \cdot \frac{\Delta I_{L2_uncoupled}}{2} \qquad \text{(E.55)}$$

So, coupling the windings while keeping the same number of turns as in the case of separate inductors results in half the ripple current amplitude for the same operating conditions (considering negligible leakage flux). This also means a coupled inductor will just require half of the inductance on each winding compared to separate inductors to keep the same winding ripple current amplitude.

Consider the previous CCM-SEPIC example, but now at 1 A load current and C_{AC} increased to around 35 µF (4 x WCAP-CSGP 885012214005 (35.2 µF, 0.6 mΩ)). Figure 33 shows the current and voltage waveforms of L_1 and L_2 when using two separate inductors (2 x 47 µH WE-PD 1050 7447714470), and Figure 34 presents the results with a coupled inductor instead, of the same winding inductance and a very-high coupling factor of k=0.995 (WE-MCRI 7448991470).

Both measurements use the same voltage and current scales for direct comparison. Observe how the voltage waveforms are the same, and with a scale of 770 mA/div, the total ripple current amplitude (i.e. $\Delta I_{L1}+\Delta I_{L2}$) has halved when using the 'high-k' coupled inductor, as expected. However, note in Figure 34 how the ripple current on each winding is not exactly the same: on L_1, it is slightly higher than half its uncoupled value, while on L_2 slightly lower. This is an example of 'unintentional' ripple current steering (explained in next section 4.2), together with the impact of a circulating loop current, as covered in section 4.3.

Figure 35 shows a circuit model for the coupled-inductor configuration of previous Figure 32, which corresponds to the common transformer 'T-model' circuit. Here, the effect of each winding's leakage flux is included in the form of winding leakage inductances, with winding-1 (L_1) assigned to the primary side, and winding-2 (L_2) to the secondary side.

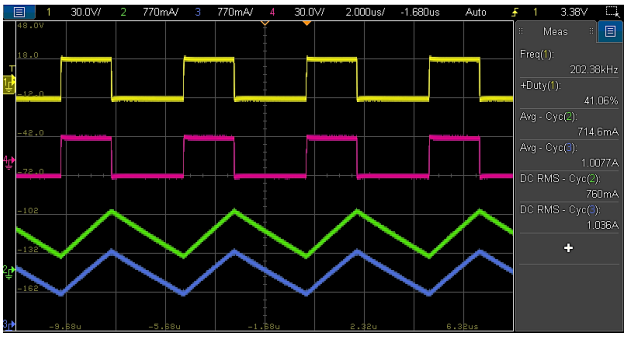

Figure 33: CCM-SEPIC measurements with two separate 47 µH inductors (WE-PD-744770147) at I_{out}=1A (I_{L1} (), V_{L1} (), I_{L2} (), V_{L2} ())

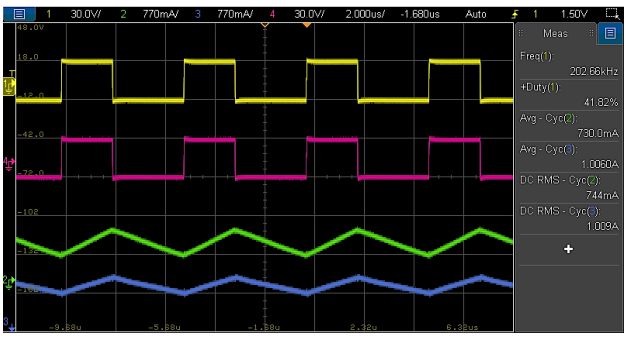

Figure 34: CCM-SEPIC measurements with a 47 µH coupled inductor (MCRI-7448991470) with k=0.995 at I_{out}=1A (I_{L1} (), V_{L1} (), I_{L2} (), V_{L2} ())

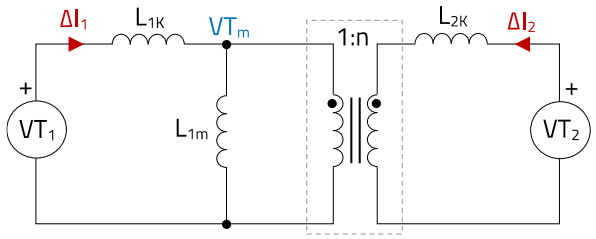

Figure 35: Voltage driven coupled inductor windings: 'T-model' circuit

Note the following:

L_{1K} – Leakage inductance of winding-1 due to $\Delta\Phi_{L1K}$

L_{1m} – Magnetizing inductance of winding-1 due to $\Delta\Phi_{L1M}$

L_{2K} – Leakage inductance of winding-2 due to $\Delta\Phi_{L2K}$

$n=N_2/N_1$ – Turns ratio

The secondary side elements can be reflected to the primary side after proper scaling by the turns-ratio, and the equivalent circuit is shown in Figure 36. Here, the two 'volt-second' sources drive a common load L_{1m} via their respective winding leakage inductances.

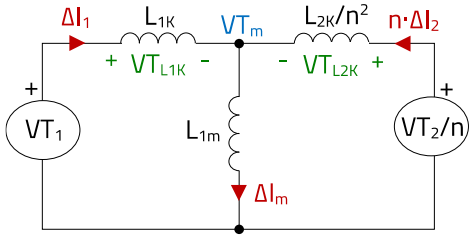

Figure 36: Coupled inductor equivalent circuit

Applying superposition, the separate contribution of each source to the volt-second across L_{1m} can be calculated. This is shown in E.56 and E.57 for VT_1 and VT_2, respectively. The total volt-second across L_{1m} is the sum of these contributions (VT_m), as per E.58.

$$VT_{m1} = \frac{1}{1+\frac{(L_{2K}+n^2\cdot L_{1m})\cdot L_{1K}}{L_{2K}\cdot L_{1m}}}\cdot VT_1 \qquad \text{(E.56)}$$

$$VT_{m2} = \frac{1}{n+\frac{(L_{1K}+L_{1m})\cdot L_{2K}}{n\cdot L_{1K}\cdot L_{1m}}}\cdot VT_2 \qquad \text{(E.57)}$$

$$VT_m = VT_{m1} + VT_{m2} \qquad \text{(E.58)}$$

The ripple current on each winding in steady-state can be obtained based on the net volt-second appearing across the respective winding leakage inductance during Δt_{on}, as follows:

$$\Delta I_1 = \frac{VT_{L1k}}{L_{1K}} = \frac{VT_1 - VT_m}{L_{1K}} \qquad \text{(E.59)}$$

$$\Delta I_2 = \frac{n \cdot VT_{L2k}}{L_{2K}} = \frac{(VT_2 - n \cdot VT_m)}{L_{2K}} \qquad (E.60)$$

Consider again the ideal case of n=1, identical windings ($L_{1K}=L_{2K}=L_K$) and equal volt-second applied to each winding ($VT_1=VT_2=V_{in}\cdot\Delta t_{on}$). These are the same conditions as in the previous example but now including the effects of the leakage flux. The equivalent circuit is shown in Figure 37.

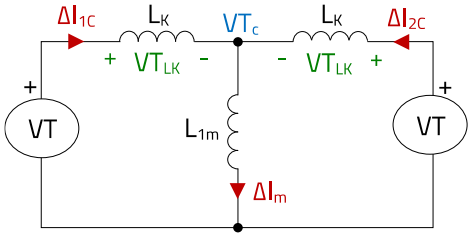

Figure 37: Coupled inductor equivalent circuit (identical windings)

From E.56 and E.57, the contribution of each source to VT_c is the same:

$$VT_{C1} = VT_{C2} = VT \cdot \frac{1}{1 + \frac{1}{k_1}} = VT \cdot \frac{k_1}{1 + k_1} \qquad (E.61)$$

In E.61, 'k_1' is the coupling coefficient related to the primary winding, defined as:

$$k_1 = \frac{L_{1m}}{L_{1K} + L_{1m}} \qquad (E.62)$$

In this case, with identical windings, 'k_1' has the same value as the total coupling factor 'k', and L_{1m} equals the mutual inductance, but this is not true in other cases.

The ripple current in one of the coupled windings is then:

$$\Delta I_{1C} = \frac{VT}{L_{1m}} \cdot \frac{k_1}{(1 + k_1)} \qquad (E.63)$$

For uncoupled inductors, the second winding is disconnected and the ripple current through the first winding (ΔI_{1U}) would be as follows:

$$\Delta I_{1U} = \frac{VT}{L_K + L_{1m}} = VT \cdot \frac{k_1}{L_{1m}} \qquad (E.64)$$

From E.63 and E.64, the ripple current ratio between the coupled and the uncoupled case in a winding is obtained:

$$\frac{\Delta I_{1C}}{\Delta I_{1U}} = \frac{1}{1 + k_1} \qquad (E.65)$$

This non-linear relationship is plotted in Figure 38.

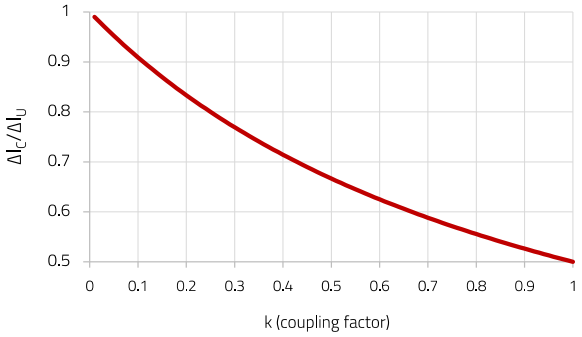

Figure 38: SEPIC: Ripple current ratio vs coupling factor

Observe how, for negligible leakage inductance (k_1~1), the ripple current ratio is 0.5, with the ripple current halving when coupling the windings, as in the previous ideal case where the leakage flux was neglected. However, as the coupling ratio decreases (i.e. leakage inductance increases), the ripple current amplitude increases, approaching the same level as in the uncoupled case as k_1 nears 0.

An LTspice™ simulation is run based on the SEPIC setup of Figure 39. Here, the coupling factor 'k' corresponds to 'k1' as used in the LTspice™ directive (identical windings). The specification is for a CCM SEPIC performing an 18 V to 12 V conversion as in the previous example, but now with a load current of 4 A, a switching frequency of 500 kHz and using 10 µH inductors, while capacitors C_{AC} and C_{out} are 100 µF and 40 µF, respectively. With D=0.42 and T_{sw}=2 µs, Q_1 on-time is calculated to be Δt_{on}=0.85 µs and the volt-second applied to each winding results in 15.3 Vµs. This would be the value assigned to the VT sources in the circuit of Figure 37.

Simulation results for k=0 (uncoupled), k=0.4 and k=0.9 are shown in Figure 40, obtaining ripple current amplitudes of 1.5 A (uncoupled), 1.1 A and around 0.78 A, respectively. Using ΔI_{1U}=1.5 A, the calculated values from E.65 for k=0.4 and k=0.9 are 1.09 A and 0.8 A, in good agreement with simulated results of Figure 40.

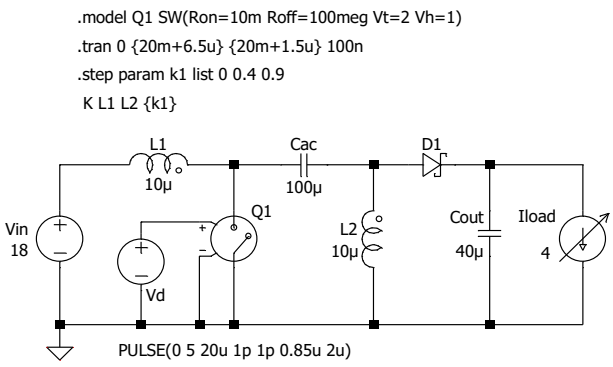

Figure 39: Coupled-inductor SEPIC setup (LTspice™ simulation)

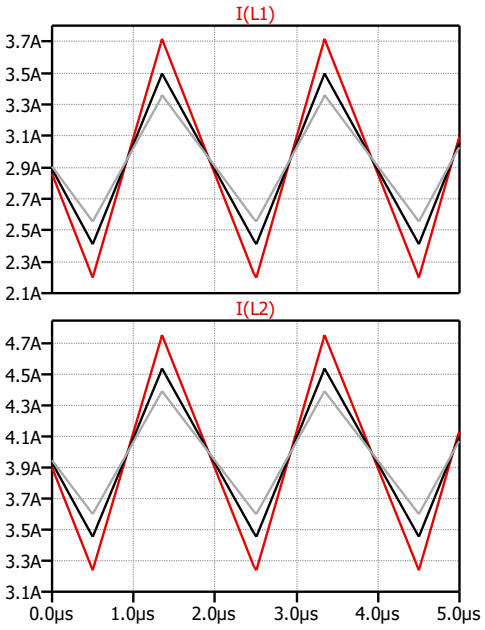

*Figure 40: LTspice™ results (k=0 (**red**), k=0.4 (**black**), k=0.9 (grey))*

4.2 Ripple current steering

In the previous example, for a set coupling factor, both windings had the same ripple current amplitude. This is because both sides of L_{1m} in Figure 37 were equal, and it can be said that the windings are 'balanced'. However, based on Figure 36, if an 'imbalance' of the windings is introduced, caused for example, by a turns-ratio other than exactly '1', different leakage flux per turn and/or volt-second applied, then the ripple current on each winding will be different.

Consider again the example specification of Figure 39, with symmetrical winding construction, the same volt-second applied, and a coupling factor of 0.9. In this case, the turns-ratio will be slightly decreased from 1 to 0.95. As both windings are structurally symmetrical, the same leakage flux per turn is generated. This means that the windings' leakage inductances can also be 'scaled' by the turns ratio.

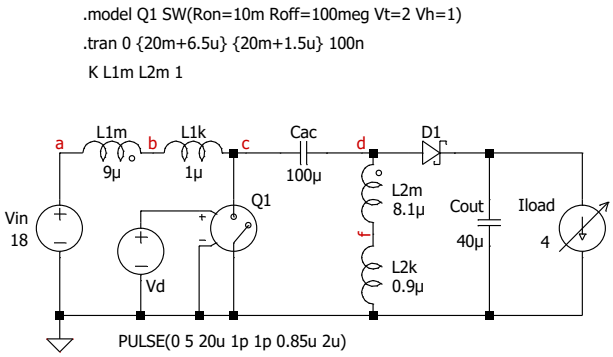

Figure 41: LTspice™ setup with discrete inductances (k=0.9, n=0.95)

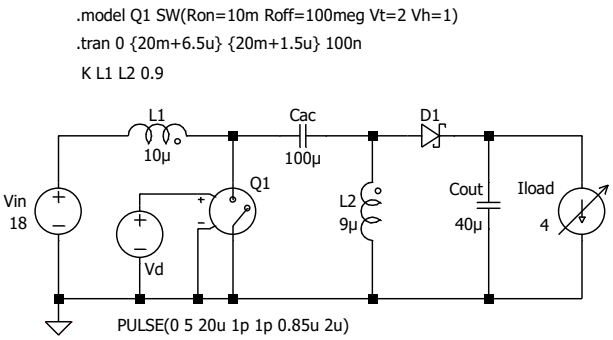

Figure 42: LTspice™ setup with 'K' directive (k=0.9, n=0.95)

With a total input winding inductance of L_1=10 µH and k=0.9, the resulting magnetizing inductance (L_{1m}) is 9 µH while its leakage inductance (L_{1k}) is 1 µH. For the second winding L_2, the magnetizing inductance (L_{2m}) is 8.1 µH and its leakage inductance (L_{2k}) is 0.9 µH, after scaling by the turns-ratio.

The equivalent simulation schematic of Figure 41 is built with discrete magnetizing and leakage inductances, allowing to observe the voltage across each of these elements. The alternative setup using the total winding inductances and coupling factor directive is shown in Figure 42, with both approaches leading to the same result. Note that the effects of windings' resistances are neglected in this analysis.

Simulation results are shown in Figure 43. The ripple current amplitude is around 0.4 A for L_1 and around 1.3 A for L_2, while the DC current levels stay unchanged as in Figure 40. Calculations for ΔI_1 and ΔI_2 from E.59 and E.60 result in 0.41 A and 1.28 A respectively, in close agreement with simulation results.

Compared to the 'balanced' case, the small 'imbalance' caused by a slightly different number of turns (N_2<N_1 in this case) has caused the ripple current in L_1 to decrease and that of L_2 to increase.

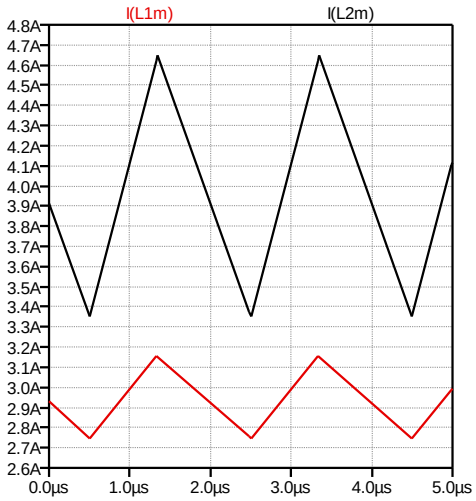

*Figure 43: LTspice™ simulation results (I_{L1} (**red**), I_{L2} (**black**))*

It is said that part of the current ripple has been 'steered' from one winding to the other.

In Figure 44, the resulting volt-seconds and ripple current amplitudes based on the T-model of previous Figure 35 are shown for this example case, as calculated from previous expressions E.56 to E.58.

The volt-second values can also be more intuitively expressed as voltages appearing across the same elements during Q_1 on-time, by just dividing these by Δt_{on}=0.85 µs. These are shown in Figure 45 together with the instantaneous voltages across the magnetizing and leakage inductances during Δt_{on}.

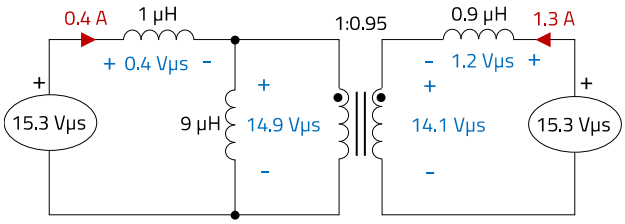

Figure 44: Calculated volt-seconds and ripple currents (k=0.9, n=0.95)

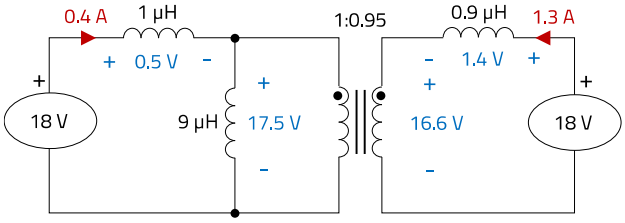

Figure 45: Calculated voltages during Δt_{on}=0.85 µs (k=0.9, n=0.95)

Simulation results are shown in Figure 46 for two switching cycles, with the schematic of Figure 41 serving as reference for the measured voltages, as follows: V(a,b) across L_{1m}, V(f,d) across L_{2m}, V(b,c) across L_{1k} and -V(f) across L_{2k}. The simulated voltages levels during Δt_{on} are around 17.45 V for L_{1m}, 16.55 V for L_{2m}, 0.5 V for L_{1k} and 1.4 V for L_{2k}, in line with calculated values on Figure 45.

Observe how, for the same voltage applied across each winding (18 V in this case), the voltage difference appearing across the primary and secondary magnetizing inductances during the on-time (~0.9 V) must be 'offset' by the voltage difference across the leakage inductances, since the volt-second applied across each winding is the same.

This condition can be expressed as:

$$V_{Lm1_on} - V_{Lm2_on} = V_{Lk2_on} - V_{Lk1_on} \qquad \text{(E.66)}$$

In a 'balanced' case, both sides of E.66 would be zero and the ripple current on the windings would be equal. An imbalance results in different voltages across the leakage inductances, which in turn, set different ripple current amplitudes as per E.59 and E.60.

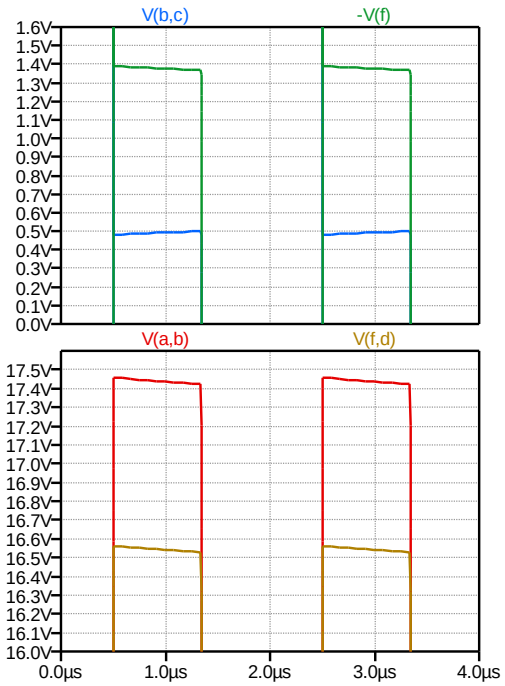

Figure 46: Simulation results: voltages across L 1k (blue), L2k (green), L 1m (red), L2m (brown), during Δt_{on}=0.85 µs showing two switching cycles (LTspice™) (k=0.9, n=0.95)

Note that this analysis is correct in this particular case as we are considering structurally symmetrical windings, where the leakage inductance is just scaled by the turns-ratio. However, even with an exact turns-ratio of '1' and for the same coupling factor, the coupled inductor could be constructed so that to make the leakage flux per turn on each winding to be different, causing with it leakage inductance imbalance and in turn, different ripple current on each winding. Note how winding imbalances can be separately introduced by the turns-ratio, the leakage inductance and volt-second applied, or a combination of them.

Although some degree of imbalance will unavoidably happen in a real design, it can also be purposely introduced to intentionally steer the ripple current amplitude from one winding to the other, in what is known as 'ripple current steering technique'.

In our SEPIC example, a reduction of the turns-ratio from 1 to 0.95 with k=0.9 led to a considerable decrease of the ripple current in the winding L_1 and an increase in L_2. However, if the turns-ratio is further reduced, the ripple current in L_1 could be eliminated altogether. The coupled inductor equivalent circuit of Figure 47 is the same as in previous Figure 35, but now showing the magnetizing inductance of L_2 instead of L_1, with:

$$L_{2m} = n^2 \cdot L_{1m} \qquad \text{(E.67)}$$

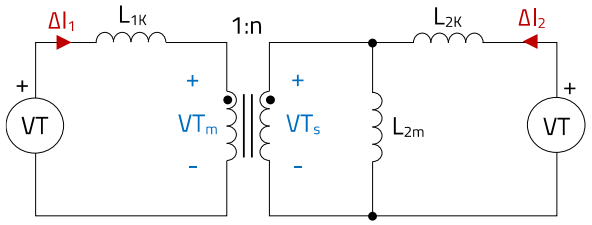

Figure 47: Coupled inductor T-model circuit (alternative version)

Considering structurally symmetrical windings:

$$L_{2k} = n^2 \cdot L_{1k} \qquad \text{(E.68)}$$

In E.62, the coupling coefficient of L_1 was defined and per analogy, the coupling coefficient of L_2 is:

$$k_2 = \frac{L_{2m}}{L_{2K} + L_{2m}} \qquad \text{(E.69)}$$

The ripple current amplitude across L_1 can be reduced to zero if the volt-second across L_{1K} is zero, leading to the following condition:

$$VT_m = VT \qquad \text{(E.70)}$$

In the circuit of Figure 47, the voltage VT_m is given as follows:

$$VT_m = \frac{VT_s}{n} = \frac{VT}{n} \cdot \frac{L_{2m}}{L_{2K} + L_{2m}} = \frac{VT}{n} \cdot k_2 \qquad \text{(E.71)}$$

From E.70 and E.71, ΔI_{L1}=0 A is achieved when:

$$n = k_2 \qquad \text{(E.72)}$$

With symmetrical winding construction, then:

$$k = k_1 = k_2 \qquad \text{(E.73)}$$

In our SEPIC example, k=0.9, and based on this analysis, the input ripple current should be zero for n=0.9. Figure 48 shows the simulation setup and Figure 49 the simulation results, confirming zero ripple current on L_1.

Note how the DC current levels stay unchanged as in previous results of Figure 40 and Figure 43, but now L_2 carries all the ripple current, with an amplitude of around 1.85 A.

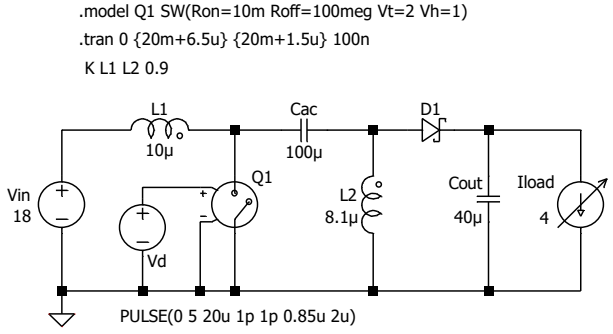

Figure 48: LTspice™ setup with K directive (k=0.9, n=0.9)

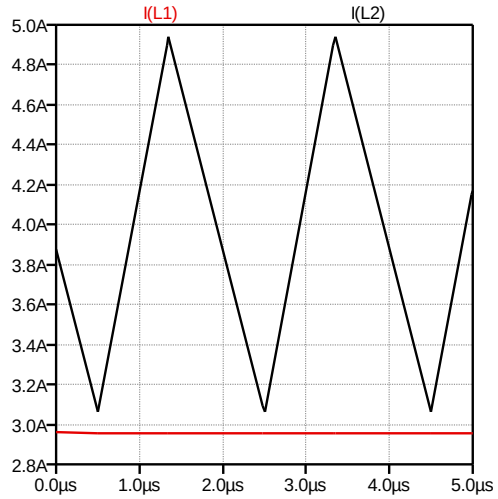

*Figure 49: LTspice™ results (I_{L1} (**red**), I_{L2} (**black**)) (k=0.9, n=0.9)*

Eliminating the converter's input current ripple is good news for conducted EMI, and this is the main advantage of using ripple current steering in a SEPIC converter.

In the examples considered so far, the turns-ratio was set higher or equal than the coupling factor. But, what would happen if the turns-ratio is now reduced from 0.9 to 0.85? The equivalent schematic with calculated volt-seconds and ripple currents is shown in Figure 50.

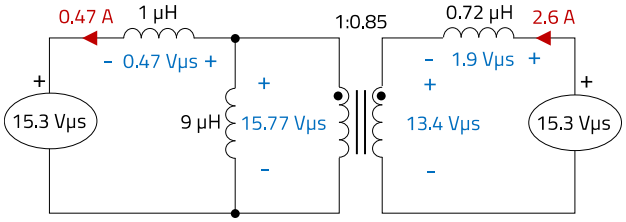

Figure 50: Calculated volt-seconds and ripple currents (k=0.9, n=0.85)

Observe how now the volt-second appearing across L_{1m} (15.77 Vµs) is higher than the total applied volt-second across the winding (15.3 Vµs). Therefore, the volt-second across the leakage inductance needs to be negative to compensate for this, which means that the voltage across L_{1K} during the on-time reverses polarity. This causes, in turn, the ripple current across L_1 to reverse direction and be now in phase with that of L_2. Note also how the voltage across L_{2K} has now increased, causing even higher ripple current through L_2 (2.6 A).

Simulation results confirm the analysis. The LTspice™ circuit setup is shown in Figure 51 and the results in Figure 52. The total ripple current amplitude combined ($|\Delta I_{L1}|+|\Delta I_{L2}|$) is now around 3.1 A, much higher than the 1.7 A from the previous case with n=0.95 (Figure 43). This shows the importance of keeping the tolerance of the imbalance introduced low when implementing ripple current steering in a SEPIC.

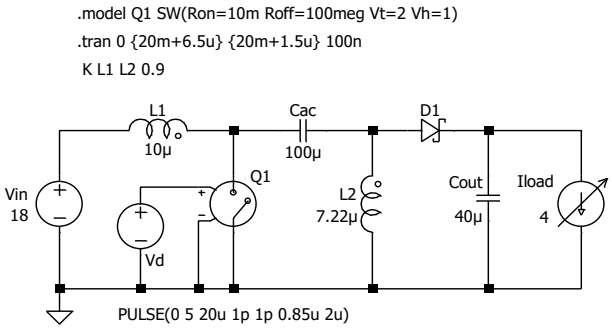

Figure 51: LTspice™ setup with K directive (k=0.9, n=0.85)

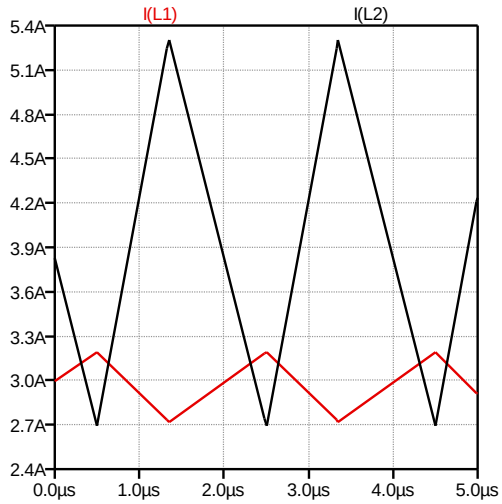

*Figure 52: LTspice™ results (I_{L1} (**red**), I_{L2} (**black**)) (k=0.9, n=0.85)*

But despite this, some input EMI filtering may still be required to cover for worst-case imbalance variations.

Note how the same zero-ripple current condition for L_1 given in E.72 can be also expressed as below:

$$\frac{N_s}{N_p} = \frac{L_{2m}}{L_{2K} + L_{2m}} \qquad \text{(E.74)}$$

E.74 provides a deeper insight, as it is expressed as a function of different physical parameters which can be adjusted in the construction of the magnetics device to set the zero ripple condition. Observe how the ripple current in one of the windings (L_1 in this case) can be reduced or eliminated by just adjusting the characteristics of the other winding (L_2 in our example).

Based on this, to reliably implement ripple current steering, a custom coupled inductor tailored for a set converter specification would be required. Power-Factor-Correction (PFC) stages and high-power DC-DC converters in SEPIC topology are normally built with custom magnetics, not only for better performance, but also due to the lack of suitable off-the-shelf parts. This allows to cost-effectively implement ripple current steering in some of these applications. Due to the high output power, they also require bulkier EMI filters, whose size and cost can be reduced when using this technique.

On the contrary, for medium and low power DC-DC SEPIC designs, off-the-shelf parts are widely available, and due to the converter input current not being discontinuous, the small EMI filter which may be required at the input may not always justify the added cost and complexity of a custom magnetics design, thus ripple current steering is not commonly implemented in such applications.

4.3 The beneficial role of leakage inductance

In the previous section, the important role of the leakage inductance when implementing ripple current steering could be understood, as it is one of the parameters which can be adjusted to create winding 'imbalance'. But additionally, E.59 and E.60 show how a higher leakage inductance could also make the system less sensitive to tolerances of the imbalance parameter(s) used, keeping the worst-case ripple current variation smaller.

Observe how in the results of Figure 40 and Figure 43, for k=0.9, the ripple current amplitude on each winding for n=1 was the same: 0.8 A. For n=0.95, ripple current amplitudes were ΔI_{L1}=0.4 A and ΔI_{L2}=1.3 A. This results in a ripple current difference of 0.4 A for L_1 and 0.5 A for L_2 between the cases of n=1 and n=0.95 with k=0.9. If a lower coupling factor of k=0.7 is now considered, the same calculations and simulations show a ripple current amplitude on each inductor of 0.9 A for n=1, while for n=0.95, ΔI_{L1}=0.8 A and ΔI_{L2}=1.1 A are obtained. This results in a ripple current variation of only 0.1 A for L_1 and 0.2 A for L_2 with k=0.7, lower than with a higher coupling factor of k=0.9.

In addition to this advantage, a high leakage inductance also helps to counteract the negative effects caused by the voltage ripple across C_{AC}, which otherwise, may considerably affect the converter's performance and reliability.

To understand this, observe the circuit loop formed by C_{in}, L_1, C_{AC} and L_2, as highlighted in Figure 53.

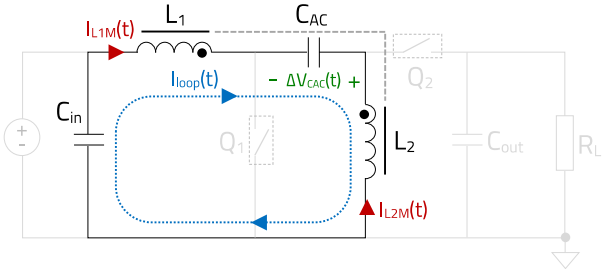

Figure 53: SEPIC circuit loop formed by C_{in}, C_{AC}, L_1 and L_2

It just contains inductive, capacitive and some parasitic resistive elements like the windings' resistances and capacitors' ESRs.

To simplify the analysis, the voltage ripple across the input capacitor (ΔV_{in}) will be considered negligible compared to that across the AC-coupling capacitor (ΔV_{CAC}), as this sustains a much higher RMS current. This voltage ripple drives an AC current in the circuit loop, referred to as $I_{loop}(t)$. On a winding, this loop current appears superimposed to the respective triangular-shaped magnetizing current ($I_{LxM}(t)$). Considering the convention for positive current direction as in Figure 53, the total instantaneous current through each winding is:

$$I_{L1}(t) = I_{L1M}(t) + I_{loop}(t) \quad (E.75)$$

$$I_{L2}(t) = I_{L2M}(t) - I_{loop}(t) \quad (E.76)$$

As it is considered that $\Delta V_{in} << \Delta V_{CAC}$, the input capacitor can be replaced by a short-circuit for AC analysis. Regarding the coupled inductor, a turns-ratio of n=1, symmetrical windings, and total leakage inductance lower than the magnetizing inductance (i.e. high coupling factor) are considered. With this, the circuit loop highlighted in Figure 53 can be approximated by the equivalent circuit of Figure 54. Observe how, for a set ΔV_{CAC}, the only elements available to limit the loop current amplitude are the leakage inductances (L_{1k} and L_{2k}) and windings' resistances (R_{L1} and R_{L2}).

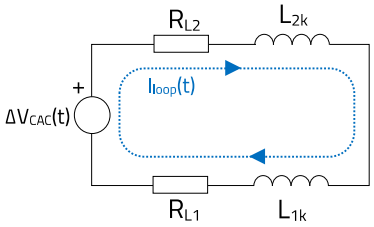

Figure 54: SEPIC equivalent circuit loop with coupled inductors (n=1)

As an example, consider ΔV_{CAC}=0.5 V and winding resistances of 50 mΩ each. If the coupled inductor had negligible leakage inductance, the resulting loop current would have an amplitude of 5 A! This current causes additional power losses in the loop's resistive elements, degrading efficiency and thermals while not contributing to the energy transfer from input to output of the converter. To avoid its negative effects, its amplitude (worst-case) should be kept at the same or lower level than that of the triangular magnetizing ripple current. But, how can this be achieved?

Considering negligible winding resistances (as it is the target for higher efficiency), the loop current is approximated as set solely by the total leakage inductance (L_{LK}), as follows:

$$I_{loop}(t) \approx \frac{1}{L_{LK}} \cdot \int_0^t \Delta V_{CAC}(t) \cdot dt \quad (E.77)$$

With:

$$L_{LK} = L_{1k} + L_{2k} \quad (E.78)$$

Note that $\Delta V_{CAC}(t)$ is a function of the current waveshape through C_{AC}, formed in turn by the combination of $I_{loop}(t)$ and the 'ideal' trapezoidal current waveform shown in previous Figure 9 (which will be referred to as $I_{CAC_ID}(t)$ here).

Considering the condition that the loop current does not dominate, and thus does not distort the ideal capacitor current (i.e. $\Delta I_{loop} < \Delta I_{CAC_ID}$), which is also the target design case, then the following approximation can be made:

$$\Delta V_{CAC}(t) \approx \frac{1}{C_{AC}} \cdot \int_0^t I_{CAC_ID}(t) \cdot dt \quad (E.79)$$

With this, previous E.77 can be now expressed as:

$$I_{loop}(t) \approx \frac{1}{C_{AC} \cdot L_{LK}} \cdot \iint_0^t I_{CAC_ID}(t) \cdot dt \quad (E.80)$$

Observe how the loop current corresponds to the double integral of a 1st order expression, resulting in a 3rd order polynomial and, therefore, of a different waveshape than the triangular magnetizing current. For a set magnetizing inductance, the amplitude of the 'ideal' trapezoidal capacitor current is just set by the converter operating conditions, so from E.80, to reduce the amplitude of the loop current, C_{AC} and/or L_{LK} must be increased. Higher C_{AC} means higher cost and PCB area required, while a higher L_{LK} can be achieved at no extra cost by simply changing the winding arrangement of the coupled inductor, as explained later. This also means that using a coupled inductor with higher leakage inductance (i.e. lower coupling factor) allows the converter to operate with less AC-coupling capacitance for the same loop current amplitude.

Based on this analysis, an approximation for the minimum AC-coupling capacitance (C_{AC}) required to set a loop current amplitude of around one-half the magnetizing current amplitude is given below:

$$C_{AC_min} \approx \frac{I_{out_max} \cdot L \cdot D_{max} \cdot T_{sw}}{2 \cdot L_{LK} \cdot V_{in(min)}} \quad (E.81)$$

Where $L=L_1=L_2$ is the total winding inductance.

To confirm this, consider the following CCM-SEPIC example specification:

V_{in} = 10 V

V_{out} = 12 V

I_{out} = 1 A

f_{sw} = 200 kHz

L : WE-MCRI 1090 7448990470 (47 µH, 220 mΩ)

C_{in} : 3 x WCAP-CSGP 885012209073 (30 µF, 1.5 mΩ)
(~ 27 µF with DC-bias)

C_{AC} : 2 x WCAP-CSGP 885012209073 (20 µF, 2.2 mΩ)
(~ 18 µF with DC-bias)

C_{out} : 2 x WCAP-CSGP 885012214005 (20 µF, 1.3 mΩ)
(~ 17.5 µF with DC-bias)

Here, the same 47 µH coupled inductor (WE-MCRI 7448990470) as for previous results of Figure 34 is used, with datasheet values of k=0.995 and L_K=370 nH (both nominal). Note how the input voltage has been decreased to 10 V, resulting in a duty-cycle of D=0.55. From this, E.81 would suggest a minimum C_{AC} of around 17 µF, and a close value of 18 µF is used.

Figure 55 shows experimental results for this configuration, with the windings currents measured based on E.75 and E.76 and the convention on Figure 53 (I_{L1} (green) at 300 mA/div and I_{L2} (blue) at 150 mA/div). Note how the otherwise purely triangular windings currents now appear slightly distorted due to the influence of the loop current. However, this is still not enough to cause the RMS currents to differ from the average current levels, and the converter still operates correctly as in the normal case.

From E.75 and E.76, the loop current is given as:

$$I_{loop}(t) = \frac{I_{L1}(t) - I_{L2}(t)}{2} \qquad \text{(E.82)}$$

In the results of Figure 55, I_{L2} is subtracted from I_{L1} using the scope's math function (violet waveform, vertical scale at 200 mA/div). From E.82, this waveform corresponds to the loop current but at twice of its real amplitude. Thus, with around 300 mA measured, the real loop current amplitude is 150 mA.

Similarly, based on the definition of E.75 and E.76, the magnetizing current on a winding is given as:

$$I_{LxM}(t) = \frac{I_{L1}(t) + I_{L2}(t)}{2} \qquad \text{(E.83)}$$

In Figure 56, again using the math function of the scope, both winding currents are added. The result corresponds to the triangular magnetizing current (violet waveform, vertical scale at 300 mA/div).

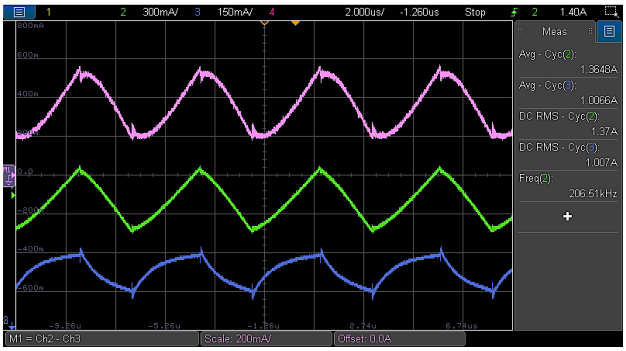

Figure 55: CCM-SEPIC measurements with WE-MCRI-7448991470 (L_K=370 nH) and C_{AC}=15 µF at I_{out}=1A (I_{L1} (), I_{L2} (), I_{L1}-I_{L2} ())

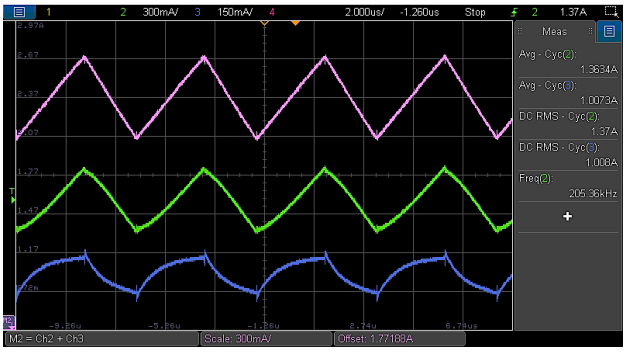

Figure 56: CCM-SEPIC measurements with WE-MCRI-7448991470 (L_K=370 nH) and C_{AC}=15 µF at I_{out}=1A (I_{L1} (), I_{L2} (), I_{L1}+I_{L2} ())

But again, this is at twice its real amplitude, as per E.83. After dividing by '2', an amplitude of around 300 mA results. This is twice as high as the measured loop current amplitude, confirming a good approximation obtained from E.81.

If C_{AC} is now reduced to 1.5 µF (i.e. by a factor of '10'), the results of Figure 57 are obtained. The now higher ripple voltage across C_{AC} generates a higher loop current, which dominates the waveshape of the measured current on each winding.

Note how the scale for both currents is set at 2 A/div, much higher than in previous Figure 55 and Figure 56, and a considerable difference between average and RMS current levels is measured.

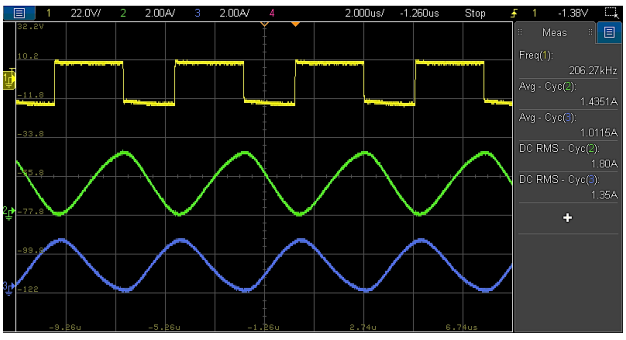

Figure 57: CCM-SEPIC measurements with WE-MCRI-7448991470 (L_K=370 nH) and C_{AC}=1.5 µF at I_{out}=1A (V_{L1} (), I_{L1} (), I_{L2} ())

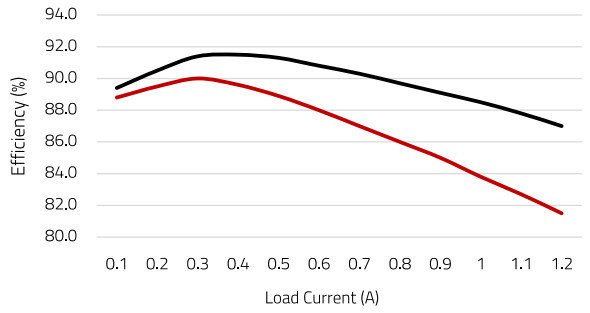

*Figure 58: CCM-SEPIC Efficiency results with WE-MCRI-7448991470 (L_K=370 nH) with C_{AC} = 1.5 µF (**red**) and C_{AC} = 15 µF (**black**)*

This has important implications for thermals and efficiency, as shown in Figure 58, where the efficiency curves for C_{AC} values of 15 µF and 1.5 µF with the same coupled inductor (WE-MCRI 7448990470) are compared. Observe how the efficiency penalty gradually increases with load current, exceeding 4 points above 1 A!

The 'high-k' WE-MCRI coupled inductor used so far is built with a bifilar winding arrangement (Figure 59 left), helping to achieve a very tight magnetic coupling. But if the winding configuration is modified, such that the primary and secondary windings are 'stacked up' as in Figure 59 right, the leakage inductance is increased while the main electrical characteristics (e.g. magnetizing inductance, DCR, rated and saturation current, etc.) remain unchanged.

Considering the same WE-MCRI 47 µH part used so far, but now using a 'stacked' winding configuration, the total leakage inductance is increased from 0.37 to 24 µH (nominal), and the coupling factor reduced from k=0.998 down to k=0.7.

The experimental results obtained with the much lower C_{AC}=1.5 µF and the 'low-k' WE-MCRI coupled inductor with stacked windings are shown in Figure 60. As advanced, the much higher leakage inductance considerably reduces the loop current amplitude, and the triangular magnetizing current now 'dominates' the measured winding currents, with almost equal average and RMS values, as in the normal case.

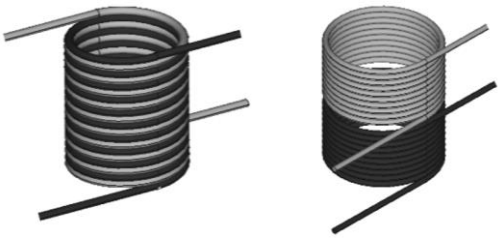

Figure 59: WE-MCRI winding variants: bifilar (left) and stacked (right)

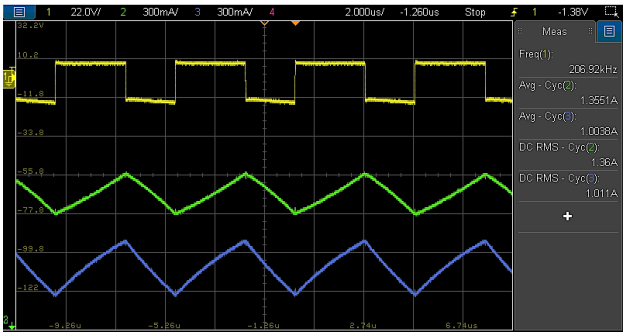

Figure 60: CCM-SEPIC measurements with WE-MCRI (L_K=24 µH) and C_{AC}=1.5 µF at I_{out}=1A (V_{L1} (), I_{L1} (), I_{L2} ())

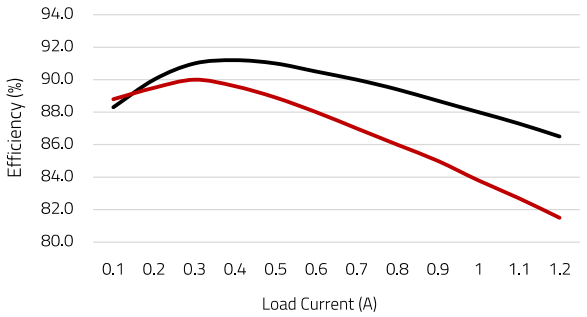

*Figure 61: CCM-SEPIC Efficiency results with C_{AC} = 1.5 µF and WE-MCRI 47 µH with k=0.995 (**red**) and k=0.7 (**black**)*

As Figure 61 shows, there is practically no efficiency penalty when reducing the AC-coupling capacitance down to 1.5 µF with the 'low-k' coupled inductor in this example. Again, over 4 points efficiency difference can be seen above a load current of 1 A compared to the case with the 'high-k' part.

Thus, helping to reduce the amount of AC-coupling capacitance without affecting the converter's performance is one of the beneficial roles of a higher leakage inductance in the SEPIC.

05. SEPIC DESIGN WITH REDEXPERT™

REDEXPERT™ is a free-to-use, online CAD tool provided by Würth Elektronik which helps designers to speed up component selection for different applications. As part of the tool, a module is dedicated to the selection of the magnetics for a SEPIC power stage, be this implemented with separate power inductors or with a coupled inductor (Figure 62).

Once the main converter specification is typed in together with the target inductor ripple current amplitude, the tool provides a list of suitable parts whose parameters and characteristic curves can be compared and filtered further based on different criteria. Amongst other things, the tool also shows the DC and AC power losses of each part from models based on real measurements.

Additional REDEXPERT™ modules relevant for SEPIC design are, for example, those of input EMI filter design or capacitor selection.

REDEXPERT™ can be accessed on this link.

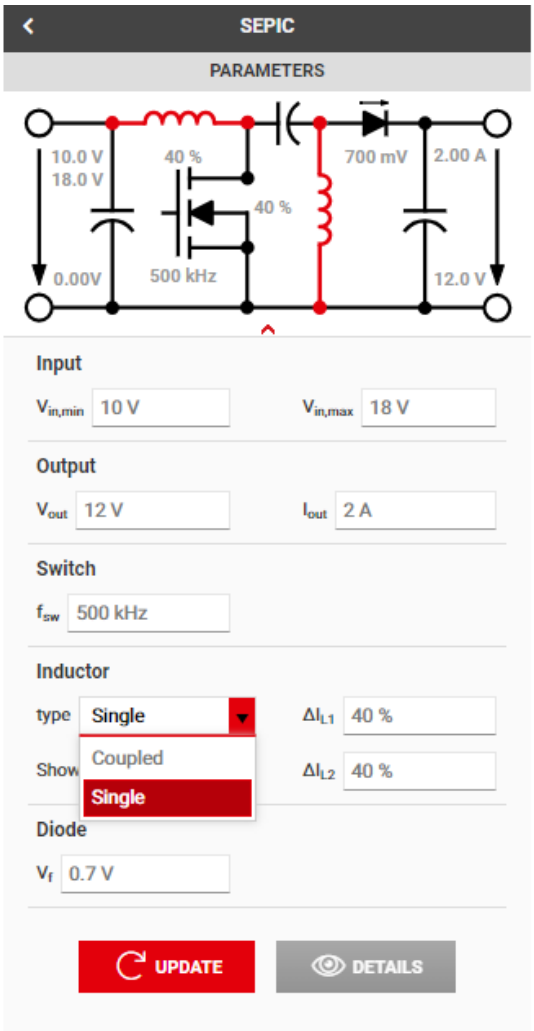

Figure 62: REDEXPERT™ module for SEPIC magnetics selection

06. WE MAGNETICS FOR SEPIC

Würth Elektronik offers a wide range of off-the-shelf magnetic components for use in switching power supplies like the SEPIC converter, be these standalone power inductors or coupled inductors with low and high coupling factors. In addition, Würth Elektronik also offers a custom magnetics design service.

6.1 Power Inductors

The range of power inductors offered by Würth Elektronik is vast. This includes shielded, semi-shielded and unshielded parts in different constructions, electrical characteristics, core materials and form factors. With REDEXPERT™, the optimal inductor for each specification and requirements can be easily identified and free samples requested for evaluation.

As a highlight, the MXGI inductor (Figure 63) is the last addition to the ever expanding range, optimized for extremely low DC and AC losses. At the date of this document, the series covers an inductance range from 0.16 to 10 µH with rated currents from 5.2 to 24.2 A. Two tiny form factors are currently offered: 4020 (4.1 x 4.1 x 2.1 mm) and 5030 (5.4 x 5.4 x 3.1 mm).

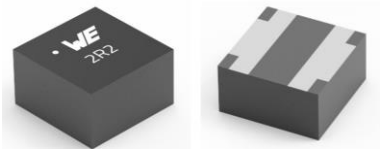

Figure 63: New WE-MXGI Power Inductor

6.2 Coupled Inductors

Würth elektronik offers various series of coupled inductors. Amongst these, the WE-MCRI (Figure 64), with a 1:1 turns-ratio, features an iron-powdered core with soft-saturation characteristic. It covers an inductance range from 1 to 47 µH and it is offered with high (k~0.995) as well as low coupling factors (currently providing free samples for evaluation).

Note that Würth Elektronik guarantees a coupling factor range for each inductance within the new 'low-k' MCRI series, helping designers to perform more accurate worst-case estimations in SEPIC, Ćuk and Zeta converters.

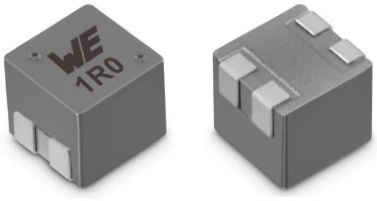

Figure 64: MCRI 1090 Coupled inductor (high and low coupling factor)

6.3 Custom Magnetics

The custom magnetics design team at Würth Elektronik supports power supply designers with the concept, design, optimization, sample build and production of tailored coupled inductors and transformers for many different topologies and applications, including the SEPIC.

As an example, Figure 65 shows a custom coupled inductor (750318760) designed for a 200 W SEPIC converter, and used in the PMP22270 reference design of Texas Instruments.

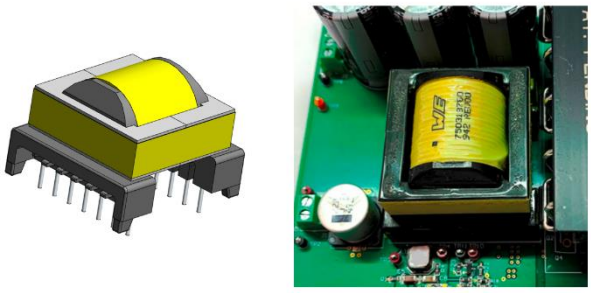

Figure 65: Example WE custom coupled inductor for a 200 W SEPIC

07. SUMMARY

In the SEPIC, the correct sizing of the AC-coupling capacitor is key for proper converter operation, and guidance for this as well as the selection of other components has been provided for both: CCM as well as DCM operation. It was seen how using a coupled-inductor instead of two uncoupled inductors can bring some advantages, like requiring less inductance for the same ripple current amplitude, or lower EMI input filter requirements when a technique known as 'ripple current steering' is implemented, both leading to potential cost savings. In addition, it has been shown how using a coupled inductor with high leakage inductance may help to reduce the amount of AC-coupling capacitance without affecting the converter performance, compared to the case of a tightly-coupled part.

In any case, whether the converter is implemented with uncoupled or coupled inductors, and this with a high or a low coupling factor, designers can take advantage of Würth Elektronik's broad product portfolio and custom magnetics capabilities for power supply designs, including the SEPIC.

A Appendix

A.1 SEPIC experimentation board

The non-synchronous SEPIC experimentation board used for the measurements in this document is shown in Figure 66. The circuit is built around the LT3757A IC current-mode controller from Analog Devices, and was designed for functional evaluation of the converter. Although the large soldering pads used for the power stage capacitors and inductors allow to easily test components of different sizes and packages (not populated in the image), they also increase undesirable parasitic elements like loops' inductances and switch-nodes' capacitances, and as a consequence, this layout is by no means optimized for EMI.

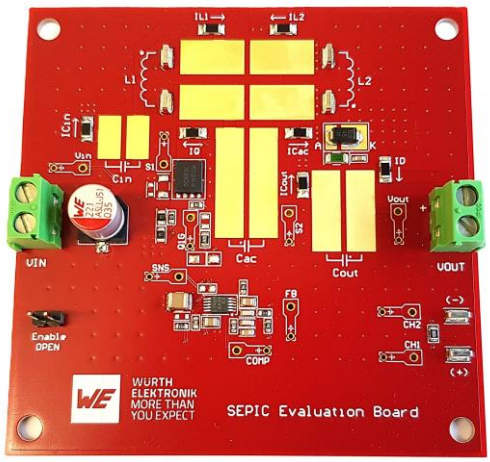

Figure 66: DC-DC SEPIC Prototype board used for measurements

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