APPLICATION NOTE #807

LVDS Clocks and Termination

ABSTRACT

This application note will highlight characteristics of Pletronics Low Voltage Differential Signal (LVDS) frequency control products and provide guidance for proper termination.

This signal type or logic type is significantly different than TTL or CMOS logic and does require special consideration to utilize the logic properly.

The terms ECL, PECL and LVPECL are reviewed.

The Application Note covers interfacing LVDS to other logic types:

- LVDS to CML
- LVDS to HSTL
- LVDS to LVDS

The importance of this logic is that it provides:

- Very high frequency operation
- Minimal EMI/RFI due to differential clock signals
- The low impedance differential outputs provide many implementation options.

The application of the Pletronics LV77, LV88 and LV99 LVDS families is reviewed.

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1 Introduction: Pletronics LVDS Output Oscillators

Hooray for standardization. Unlike its cousins from other logic families, LVDS is standardized. Standards bodies define LVDS in specification ANSI/TIA/EIA-644A. Logic families such as Low-Voltage Positive Emitter Coupled Logic (LVPECL) and Current-Mode Logic (CML) are widely used but neither technology has been standardized by any official standards organization. Implementation of these logic families is vendor specific so a careful specification review is important.

1.1 History of LVDS

National Semiconductor first introduced LVDS as a standard in 1994. National recognized that the demand for bandwidth was increasing at an exponential rate while users also desired low power dissipation. The demands exceeded the speed capabilities of RS-422 and RS-485 differential transmission standards. While Emitter Coupled Logic (ECL or PECL) was available at the time, it can be difficult to interface with standard logic levels.

Output	LVDS	PECL 3.3V	PECL 2.5V
V_{OH} (Minimum)	1.249 V	2.27 V	1.47 V
V_{OL} (Maximum)	1.252 V	1.68 V	0.88 V

The LVDS levels do not change with supply voltage.

The PECL output levels follow the supply voltage. The values shown are for the nominal supply voltage only.

Input	LVDS	PECL 3.3V	PECL 2.5V	HSTL	CML
V_{REF} or V_{CM}	1.20 V	2.00 V	1.20 V	0.75 V	V_{CC} - 0.40 V
V_{ID} (Minimum)	200 mV	310 mV	310 mV	400 mV	400 mV
V_{IH} (Minimum)	1.249 V	2.27 V	1.47 V	V_{REF} + 0.2 V	V_{CC}
V_{IL} (Maximum)	1.252 V	1.68 V	0.88 V	V_{REF} - 0.2 V	V_{CC} - 0.40 V

Some of the advantages of LVDS are:

- Lower power than other technologies
- Output signal that is power supply independent
- Low voltage power supply compatibility
- Low generation of noise (EMI/RFI)
- High noise rejection
- Reliable signal distribution
- Ability to drive longer line lengths than CMOS

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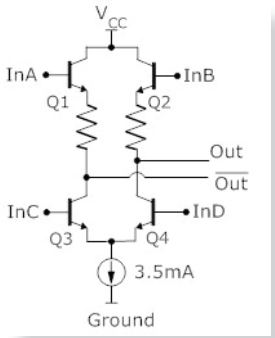
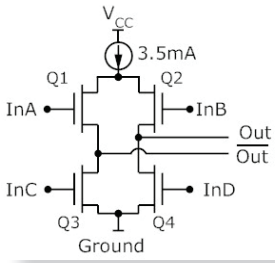
1.2 About LVDS Drivers

The LVDS output is essentially “H Bridge” type driver. This can be realized with MOS or BJT devices.





The termination is 100 ohms connected between the Out and Out*. The InX nodes are driven from the internal circuitry. The output states are:

Output	Q1	Q2	Q3	Q4	Out	Out*	Output
Logic 1	Off	On	On	Off	+3.5 mA	-3.5 mA	+350 mV
Logic 0	On	Off	Off	On	-3.5 mA	+3.5 mA	-350 mV

1.3 What differentiates the Pletronics LV7, LV8 and LV9 series clock oscillators?

Pletronics provides an assortment of LVDS output solutions. These solutions all meet the ANSI/TIA/EIA-644 LVDS specification, but differ in the method of achieving the output frequency. The VPU7 VCXO family has the same characteristics as LV9.

Characteristics	LV7	LV8	LV9
Crystal Mode Used	3rd Overtone	Fundamental	Fundamental
Frequency Range	80 to 325MHz	106.25MHz and 212.5MHz only	10.9MHz to 700MHz
Supply Voltage	1.8V, 2.5V and 3.3V	3.3V	3.3V
Multiplication Method	none	Low Noise PLL with an LC VCO phase locked to the crystal	Low Noise PLL with an LC VCO phase locked to the crystal
Process Technology	BiCMOS	RF SiGe BiCMOS	RF SiGe BiCMOS
Phase Noise	Inclose phase noise excellent	---	---
Jitter	Excellent	Good	Good
Tr and Tf	Good	Good	Excellent (very fast)

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2 Interfacing LVDS Outputs to Other Logic Inputs

From time to time, it may be necessary to support other logic families. Pletronics supplies a wide assortment of CMOS and LVPECL oscillators. For those applications, it is only necessary to select the correct device. Basic termination of LVDS is covered along with examples of how to terminate to other logic types.

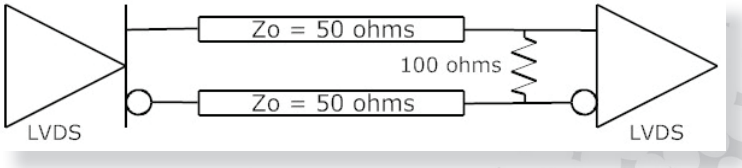
Pletronics provides specification compliant LVDS products in 5x7mm (LV77 series) and 3.2x5mm (LV55 series) Crystal Oscillators (XO) and 5x7mm Voltage Controlled Crystal Oscillators (VCXO) (VLU7 series). Frequencies are available from 1MHz to 670MHz in commercial (-10 to +70oC) or industrial (-40 to +85oC) temperature ranges. Pletronics manufactures LVDS devices with supply voltages of 3.3v, 2.5v and 1.8v.

Termination of specification compliant LVDS devices is simple. The termination network is a single 100-Ohm resistor across the receiver input. Unlike LVPECL, LVDS receivers have a wide common mode range so they are effectively power supply agnostic. Devices with power supply voltages of 3.3v, 2.5v and 1.8v interoperate without the need for special termination gymnastics or AC coupling.

AC coupling options are shown but one must then remember there is a low frequency limit that must be observed. The low frequency limit is set by the capacitor values and associates resistors.

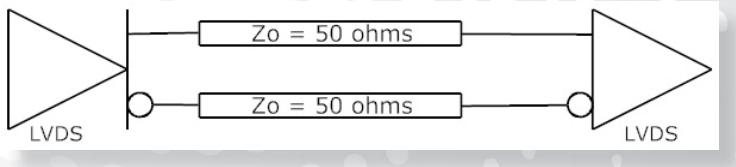
2.1 Interface LVDS to LVDS with Termination On the PCB

A single 100 ohm terminating resistor placed at the end of the signal path is all that is needed. The end of the path is after the pads to the destination LVDS inputs.



2.2 Interface LVDS to LVDS with Termination Internal in the Destination IC

This is the simplest of all configurations and with the termination internal to the receiving device results in the best signal integrity. Many of the FPGAs permit this option to be



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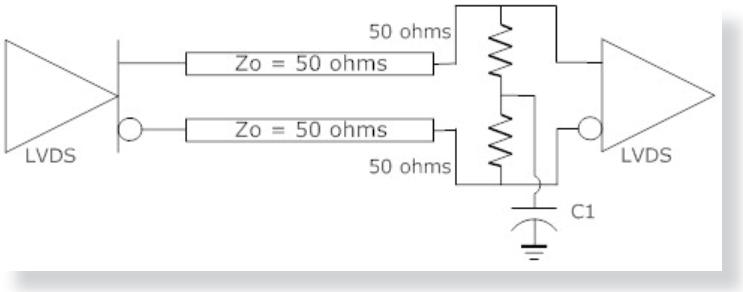
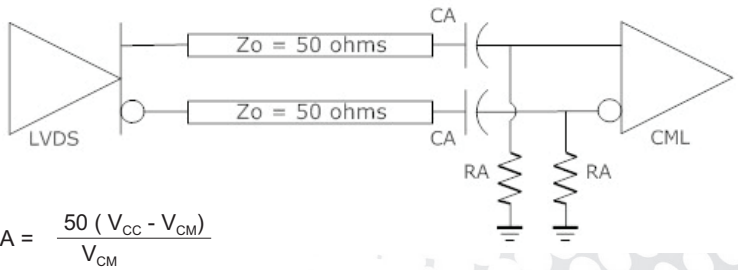
2.3 Interface LVDS to LVDS with Termination Split and a Capacitor

The designer could split the 100 ohm termination resistor into two 50 ohm resistors, resulting in a node in the middle of the termination that, if all is balanced, is 1.2V DC. To terminate any unbalanced noise within the differential transmission line as well as correct for any line length mismatches, a capacitor (C1) can be placed from this balanced node to ground. A recommended value is 0.01uF made with X7R dielectric.



2.4 Interface LVDS to CML

Pletronics does not supply CML specific devices. Instead, it is possible to connect an LVDS oscillator directly to CML logic. Since CML inputs incorporate termination resistors and in many cases the bias voltage the only external components required are the two coupling capacitors (CA) and optionally two resistors (RA) to set VCM if the internal bias is not set. This example does assume the CML internal termination is 50 ohms.



$$RA = \frac{50\ (V_{CC} - V_{CM})}{V_{CM}}$$

$V_{CM} = 0.20$ V

Condition	RA (ohms)
Internal V_{CM} bias	None
V_{CC} = 5.0V	1200
V_{CC} = 3.3V	775
V_{CC} = 2.5V	575
V_{CC} = 1.8V	400

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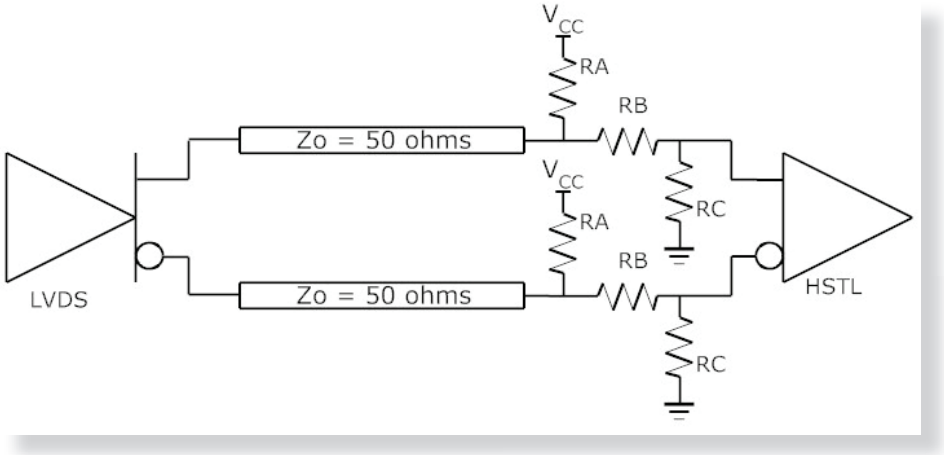
As mentioned earlier, CML is not standardized so vendor-to-vendor differences may and do exist. If the CML receiver lacks one or both of these, an external resistor network will be required. Consult the receiver's data sheet for recommendations.

2.5 Interface LVDS to HSTL

The interface to HSTL is more complicated for the DC connection case. This requires matching the impedances, level shifting the LVDS signal while maintaining the proper bias levels on the LVDS driver.



The resistor values must meet these criteria

$$\frac{V_{CM}}{V_{CC}} = \frac{RB + RC}{RA + RB + RC}$$

$$\frac{V_{REF}}{V_{CC}} = \frac{RC}{RA + RB + RC}$$

RA // (RB + RC) = 50 (terminating resistance of LVDS)

V_{CM} = 1.2 for LVDS

V_{REF} = 0.75 for HSTL

Solving the equations results in these values.

V_{CC} (V)	RA (ohms)	RB (ohms)	RC (ohms)
3.3	140	30	50
2.5	100	36	60

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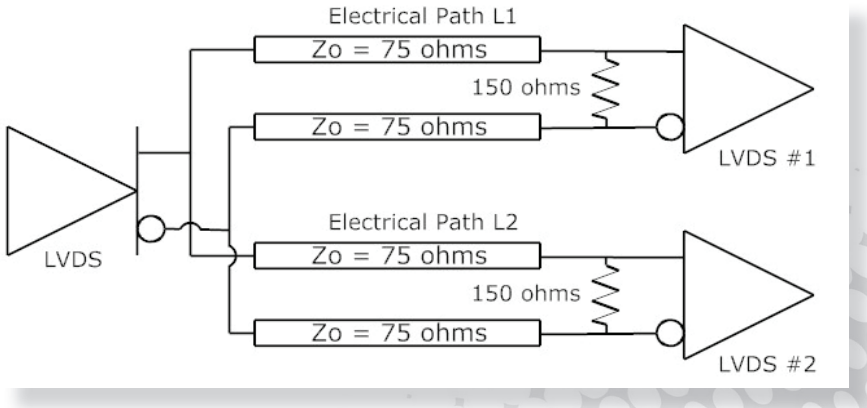
2.6 Example of Driving 2 LVDS inputs with no clock skew

The LVDS output is flexible and variations can be used. The requirement and conditions are:

- LVDS clock needed to drive two LVDS devices
- The LVDS receivers permitted external terminating resistors
- The should be no clock skew between the two receivers
- Adding an LVDS buffer and the resulting jitter addition was a concern
- Board space and power was at a premium

The minimum level of the LVDS receivers is such that a somewhat attenuated signal will work properly. There is no reason that 50 ohm loads are needed on the transmission lines. In this case 75 ohm terminations were chosen. This results in the LVDS signal being attenuated by 25%.

The LVDS clock was placed between the two LVDS receivers, the 150 ohm termination resistors were placed at the end of each path. Then making the 'Electrical Path L1' the exact same as 'Electrical Path L2' solved the required clock skewing be zero.



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