

ESD: Kill or Be Killed

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You can either protect sensitive circuits from ESD damage or let ESD ruin your product, your day, and even your job.

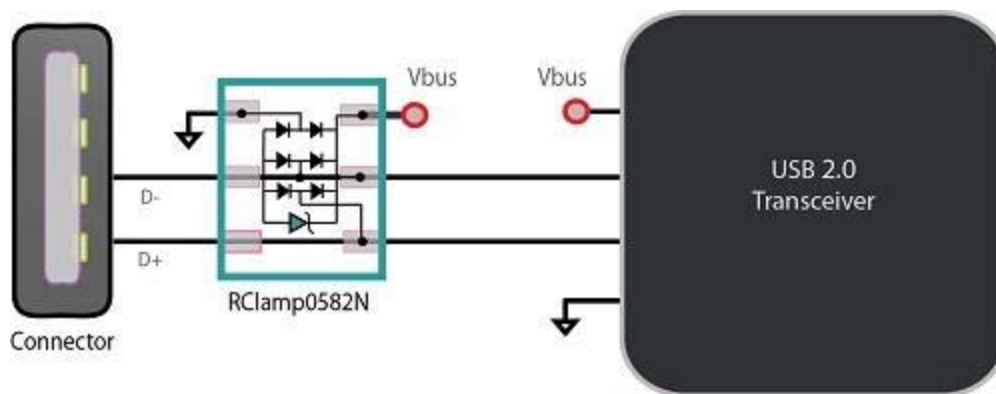
Microelectronic circuits are in more peril than ever before. The culprit: ESD (electrostatic discharge). These zaps are stealthy killers with an affinity for attacking sensitive ICs. A single ESD event can send PCBs to the graveyard. A misstep in the ESD immunity design can mean lost time to market, impacted schedules, anxious management, and angry customers. And, in some high pressure cases, it might mean your job.

In the age of ever-shrinking microelectronics, system designers need to adopt a new product compliance motto: Kill or be killed. In other words, if you don't proactively plan to kill ESD transients before they run unchecked on your PCB traces, there's a good chance that an ESD event will kill your product.

Along these lines, I had a rather interesting experience a few months ago. A frantic customer contacted us for some eleventh-hour help in protecting his system against some "angry" ESD transients. This poor fellow was basically ambushed by a series of ESD immunity failures that had sent his product schedule into a tailspin. There were definitely a few missteps.

First, he didn't implement protection clamps at any of the I/O interfaces, nor did he place PCB pads for TVS clamps as a "safety valve" move should he need protection. To compound the challenge, the I/O ports on this particular product were connected to some high-speed and very sensitive communication ICs. It didn't take much of an ESD zap to send these boards out of commission. **Figure 1** shows an example of using clamping diodes on a data line.

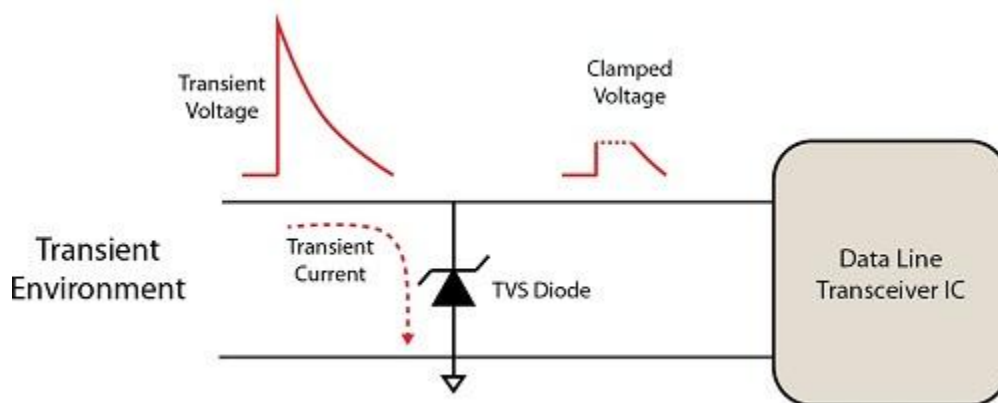
Figure 1



TVS diodes provide ESD protection across data lines. The example here shows USB 2.0 data lines with ESD protection.

When the first board failed the ESD compliance test, out went rev. 1 and in came rev. 2. This time, it was a little bit less of a "shot in the dark." The customer -- good for him -- had apparently found a TVS (transient-voltage-suppression) clamp with an ESD rating to ± 15 kV. He sprinkled a few of these at the I/O ports of his board and rather happily assumed that this part guaranteed him a robust ± 15 kV ESD immunity for his system. While it was a step in the right direction, he still had a basic misunderstanding of the ESD threat. The rev. 2 board spin still failed well below ± 15 kV test voltage, though at this point he had seen some modest improvement with the TVS. **Figure 2** shows how a TVS diode can "clamp" voltages from ESD pulses.

Figure 2



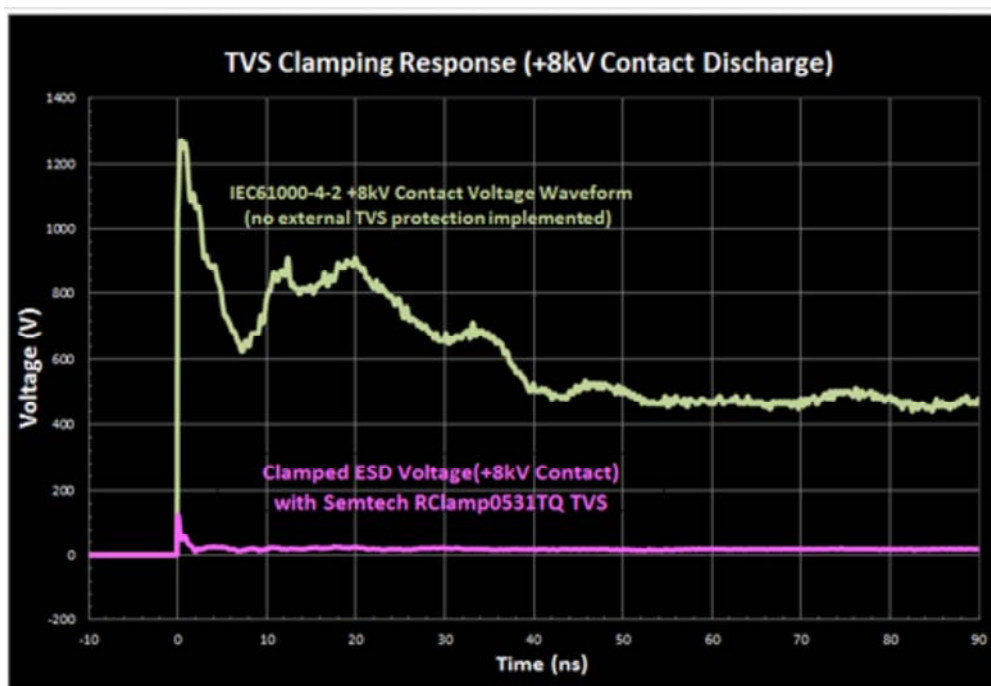
Clamping diodes can reduce the voltage from an ESD pulse, which can save your circuit from damage.

With two strikes against him, the engineer turned to us in a panic. As we talked through the issues, I really felt this engineer's angst. In fact, I got the distinct impression that the ESD transients running amok on his PCB traces not only threatened to kill the communication ICs on his board, they literally threatened to kill his job. He needed a solution yesterday. With the clock ticking and a big, impatient customer on the other end of this late design, we took over. He sent his boards to our Semtech lab with the clear objective of safeguarding the product from ESD and, with it, his credibility and, perhaps, job.

The misunderstanding that we needed to dispel, however, was that the ± 15 kV rating on the device datasheet of the TVS clamp has little to do with the system-level protection threshold he would achieve on his PCB. That rating applies to the failure threshold of the TVS device itself, but doesn't imply the immunity level guaranteed to the system. As it was, his system

circuit was so sensitive that with the capacitance constraints and size requirements for the TVS part, achieving ± 15 kV of system-level immunity was going to be very difficult.

What's more, we explained that not all TVS devices are created equal. There can be a wide variation in clamping performance between two TVS clamp devices from different manufacturers. When tight product schedules are on the line, choosing cheap, copycat TVS devices is a bad strategy. So, we retrofitted his board with some newer, high-performance, lower clamping devices -- devices highly engineered to squash the high peak current. With that, there was marked improvement in the ESD immunity, as the plot below shows.



Adding transient voltage suppression can significantly reduce clamping voltage, protecting sensitive ICs.

His system now comfortably passed ± 8 kV at this point (and for most, ± 8 kV is sufficient). The board was still not passing ± 15 kV contact discharge (a stretch objective), but it was much better than the previous results. From there, to increase the system robustness, we added a small series resistance on the line, enough to squelch residual transient current, but not significant enough to impact the signal performance.

While adding the resistance was not ideal, it bolstered the ESD immunity, and at such a late stage in the design cycle it provided a rather easily implementable fix. In the end, it all turned out well: a robust product, a happy end-customer, a pleased boss, and an engineer with a deeper understanding of ESD protection fundamentals. As they say, "An ounce of prevention is worth a pound of cure." I would guess that on his next design, our friend will be a lot more proactive to avoid any eleventh-hour ESD miscues.

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